KAWA ELECTRONIC RESEARCH & DEVELOPMENT CENTRE

Service Manual

Reference No. : SM- PDP50HADSE-001
Revision : 0
Date : 2006.Nov.
Page : P.1 of 96

In House Model No. : PDP50HAD
Customer Model No. : PDP5016H

BOM No : PDP50HADSE–A01

Description : Service Manual for PDP5016H_S50HW-XD03_USA

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Approved By: Engineering Manager

Received By: MK Department

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0	Initial Release	2006-Nov-21

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SERVICE MANUAL

Model: PDP5016H

This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

Safety Precaution

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

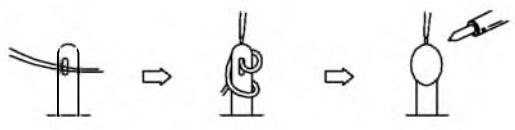
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated “dangerous voltage” within the product’s enclo sure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
   Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

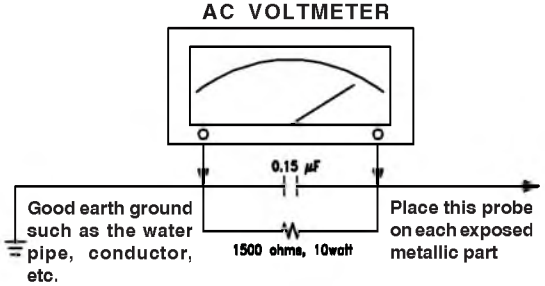
Before servicing this TV receiver, read the SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads,metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.
   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15μF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.
   The measured voltage must not exceed 0.3V RMS.
   This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.
   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

Technical Specifications	MODEL : *PDP-5016* 50" Plasma Display			
DATE FIRST ISSUED	ISSUE 1	RAISED BY	CHECKED BY	NUMBER OF PAGES 9

REVISIONS

ISSUED	DATE	DESCRIPTION	RAISED BY :

SPECIFICATION AGREED :	SIGNATURE	DATE
R & D DEPARTMENT	.....	.....
COMMERCIAL DEPARTMENT	.....	.....
PRODUCTION DEPARTMENT	.....	.....
Q/A DEPARTMENT	.....	.....
CUSTOMER	.....	.....
	.....	.....

SPECIFICATION APPROVED : SIGNATURE : DATE :

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NOTE :	Only documents stamped "Controlled Document" to be used for manufacture of production parts.

1. Standard Test Conditions

All tests shall be performed under the following conditions, unless otherwise specified.

1.1	Ambient light	:	150ux (When measuring I_B, the ambient luminance $\leqq 0.1Cd/m^2$)
1.2	Viewing distance	:	50cm in front of PDP
1.3	Warm up time	:	30 minutes
1.4	PDP Panel facing	:	no restricted
1.5	Measuring Equipment	:	PC, Chroma 2225 signal generator (with Chroma digital additional card) or equivalent, Minolta CA100 photometer
1.6	Magnetic field	:	no restricted
1.7	Control settings	:	Brightness, Contrast, Tint, Color set at Center(50)
1.8	Power input	:	100~240Vac
1.9	Ambient temperature	:	20°C ± 5°C (68°F ± 9°F)
1.10	Display mode	:	31.5KHz/60Hz (Resolution 1366 x 768)
1.11	Other conditions	:	

1.11.1 With image sticking protection of PDP module, the luminance will descend by time on a same still screen and rapidly go down in 5 minutes. When measuring the color tracking and luminance of a same still screen, be sure t o accomplish the measurement in one minute to ensure its accuracy.

1.11.2 Due to the structure of PDP, the extra-high-bright same screen should not hold over 5 minutes for fear of branding on the panel.

ELECTRICAL CHARACTERISTICS

2. Power Input

2.1	Voltage	:	100 ~ 240VAC
2.2	Input Current	:	5.0 /2.5A
2.3	Maximum Inrush Current	:	<30 A (FOR AC110V ONLY)
	Test condition	:	Measured when switched off for at least 20 mins
2.4	Frequency	:	50Hz to 60Hz(±3Hz)
2.5	Power Consumption	:	≤ 480W
	Test condition	:	full white display with maximum brightness and contrast
2.6	Power Factor	:	Meets IEC1000-3-2
2.7	Withstanding voltage	:	1.5kVac or 2.2kVdc for 1 sec

3. Display

3.1	Screen Size	:	50" Plasma display
3.2	Aspect Ratio	:	16:9
3.3	Pixel Resolution	:	1366x768
3.4	Peak Brightness	:	1000 cd/m² (Panel module without filter)
3.5	Contrast Ratio (Dark room)	:	4000:1 (Panel module without filter)
3.6	Viewing Angle	:	Over 160°
3.7	OSD language	:	English

4. Signal

4.1 TV/AV & Graphic input

4.1.1 TV standard	:	NTSCM,PAL/N,PAL/M
4.1.2 TV Tuning system	:	PLL 181CH
4.1.3 CATV	:	125CH
4.1.4 Composite signal	:	CVBS
4.1.5 Y,C Signal	:	S-Video
4.1.6 Component signal	:	Y, Pb/Cb, Pr/Cr, HDTV compatible
4.1.7 Graphic I/P	:	Analog: D-sub 15pin detachable cable Digital: DVI
4.1.8EDID compatibility	:	DDC 1.3
4.1.9 I/P frequency	:	f_H: 31.5kHz to 60kHz/f_V: 56.25Hz to 75Hz (1024X768 recommended)

4.2 Audio input

Audio I/P(L/Rx5) : 1 for DVI / D-Sub
1 for Y/ Pb/Pr
1 for Y/ Cb/Cr
1 for CVBS
1 for S-Video

4.3 AV output

Audio&Video O/P(RCAx3) : Monitor out(Video & Audio L/R)

4.4 Other function : PIP/POP/PBP, Picture size, Picture Still, Sound mode,Last memory, Timer, MTS

5. Environment

5.1 Operating environment

5.1.1 Temperature : 5º to 33°C

5.1.2 Relative humidity: 20% to 85%(non-condensing)

5.2 Storage and Transport

5.2.1 Temperature : -20°C to 60°C(-4º to 140°F)

5.2.2 Relative humidity: 5% to 95%

6. Panel Characteristics

6.1 Type : S50HW-XD03

6.2 Size : 50", 1190mm(width)x7005mm(height)x59mm(depth)±1 mm)

6.3 Aspect ratio : 16:9

6.4 Viewing angle : Over 160°

6.5 Resolution : 1366X768

6.6 Weight : 22.0kg ±0.5 kg (Net)

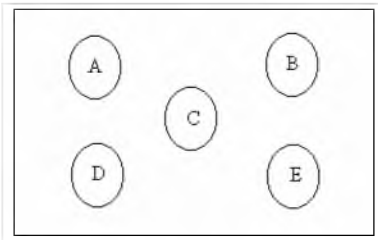
6.7 Color : 1024(R)X1024(G)X1024(B) COLORS

6.8 Contrast : Average 60:1 (In a bright room with 150Lux at center)
Typical 5000:1 (In a dark room 1/100 White Window pattern at center).

6.9 Peak brightness : Typical 1000cd/㎡ (1/25 White Window)

6.10 Color Coordinate Uniformity : Contrast; Brightness and Color control at normal setting

Test Pattern : Full white pattern



Average of point A,B,C,D and E +/- 0.01

6.11 Color temperature : Contrast at center (50); Brightness center (50);
Colortemperature set at Natural
x=0.285±0.02
y=0.290±0.02

6.12 Cell Defect Specifications
Subject to Panel supplier specification as appends.

7. Front Panel Control Button

7.1 CH Up / Down Button : Push the key to changing the channel up or down.
When selecting the item on OSD menu.

Volume Up/ Down Button : Push the key to increase the volume up or down.
When selecting the adjusting item on OSD menu
increase or decrease the data-bar.

Menu Button : Enter to the OSD menu.

Source Select Button : Push the key to select the input signals source.

7.2 Stand by Button : Switch on main power, or switch off to enter power
Saving modes.

7.3 Main Power Switch : Turn on or off the unit.

8. OSD Function

8.1 Picture : State (Normal,Dark,Bright,User); Display (Bright,contrast,Color,Hue)
Temp (warm,Cool,Normal,User);
Position (H-posit,V-posit,Phase,H-size,Auto Adjust)

8.2 Sound : Setup (Mode,AVC,Volume,Balance);
Equalizer (120HZ,500HZ,1.5KHZ,5KHZ,10KHZ)
BBE Setup (Gain,Treble,Bass)

8.3 OSD : Size (Panorama,16:9,Normal,Anamorphic,Letter Box,TV Mode)
OSD Set (Language,OSD Position,Time Out)
Option (Burn Protect, Version)
V-Chip , C/C

8.4 Layout : Layout (Full Screen,PIP,Split Screen,Grid,POP 3,POP 12)
PIP Set (Sub Win Source,Sub Win Size,PIP Size.PIP Position)

8.5 Time : Sleep (30Min,60Min,90Min,120Min,180Min)
Wake Up (Time Edit,Volume,TV Mode,Channel)
Time Set

8.6 TV Set : TV Set (Auto Search,Manul Search,System,MTS,Auto Fine,Fine)
CH Edit

9. Agency Approvals

Safety	UL60950
Emissions	FCC class B

10. Reliability

11.1 MTBF : 20,000 hours(Use moving picture signal at 25°C ambient)

11. Accessories : User manual x1, Remote control x1, Stand x1, Power cord x1, Battery x 2, Accessories box x 1,Speaker x 2,Speaker wire x2

12. Support the Signal Mode

A. D-Sub Mode (VGA or DVI)

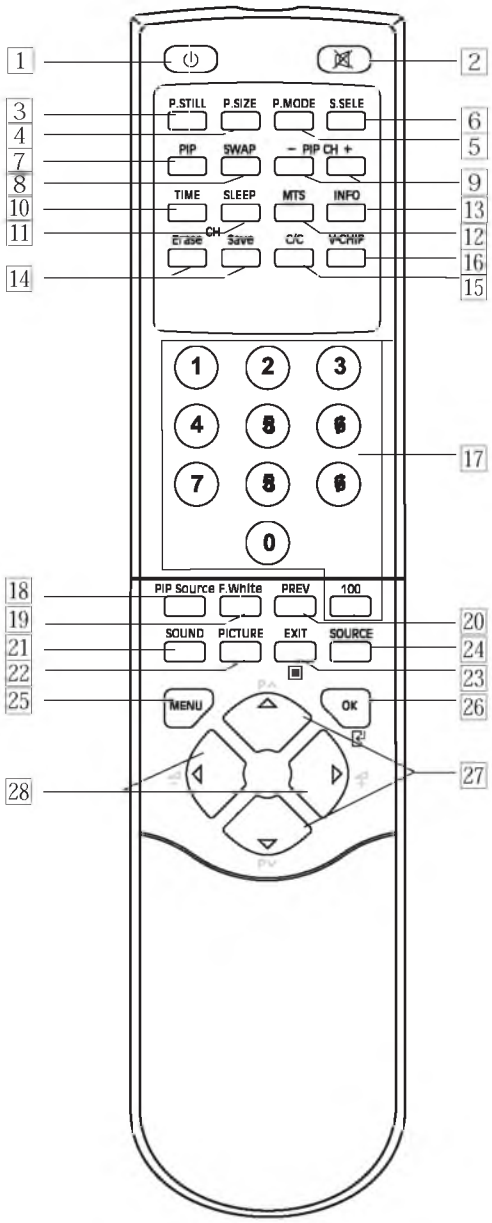
NO.	Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Dot Clock Frequency (MHz)
1	640 x 400	31.47	70.08	25.17
2	640 x 480	31.50	60.00	25.18
3	640 x 480	35.00	67.00	30.24
4	640 x 480	37.50	75.00	31.50
5	640 x 480	37.86	72.81	31.50
6	720 x 400	31.47	70.08	28.32
7	800 x 600	35.16	56.25	36.00
8	800 x 600	37.90	60.32	40.00
9	800 x 600	46.90	75.00	49.50
10	800 x 600	48.08	72.19	50.00
11	832 x 624	49.00	74.00	57.27
12	1024 x 768	48.40	60.00	65.00
13	1024 x 768	56.50	70.00	75.00
14	1024 x 768	60.00	75.00	78.75
15	1152 x 864	54.53	61.13	80.37
16	1152 x 864	63.86	70.02	94.51
17	1152 x 864	67.52	75.02	108.03
18	1280 x 960	60.02	60.02	108.04
19	1280 x 1024	64.00	60.01	108.00

B. DTV Mode

NO.	Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Dot Clock Frequency (MHz)
1	480 i	15.734	59.94	13.50
2	576 i	15.625	50.00	13.50
3	480p(720x480)	31.468	59.94	27.00
4	576p(720x576)	31.25	50.00	27.00
5	720p(1280x720)	45.00	60.00	74.25
6	720p(1280x720)	37.50	50.00	74.25
7	1080i(1920x1080)	28.125	50.00	74.25
8	1080i(1920x1080)	33.75	60.00	74.25

- When the signal received by the Display exceeds the allowed range, a warning message “Out Of Range” shall appear on the screen.
- You can confirm the input signal format from the “OSD Menu”.

13. Remote Control



1. **Power (⏻)**: Press to turn on and off.
2. **Mute (🔇)**: Press to mute the sound. Press again or press ▶ to restore the sound.
3. **P.STILL**: Press to freeze the picture. Press again to restore the picture.
4. **P.SIZE**: Press to cycles through the picture size: Normal, Fill Screen, Anamorphic, Letter Box or TV Mode, Panorama..
5. **P. MODE**: Press to cycles through the picture mode: Normal, Bright, Dark, User.
6. **S.SELE**: Press to cycles through the sound select: Main window sound or Sub window sound.
7. **PIP**: Press to turns on PIP (picture-in-picture) feature. Such as Full Screen, PIP or Split Screen.
8. **SWAP**: Press to switches the Main window or Sub window pictures.
9. **PIP CH+** : Press to select Sub window Channel Up.
   PIP CH- : Press to select Sub window Channel Down.
16. **TIME**: Press to display the current time.
11. **SLEEP**: Press repeatedly until it displays the time in minutes (30 Min, 60 Min, 90 Min, 120 Min, 180 Min or Off) that you want the PDP to remain on before shutting off. To cancel Sleep Time, press SLEEP repeatedly until Sleep Off appears. And you can press ◀ or ▶ to select sleep time shut down.
12. **MTS**: Press repeatedly to cycle through the Multi-channel TV sound (MTS) options: Mono, Stereo and SAP (Second Audio Program).
13. **INFO**: Press to display on-screen information. Press it again to turn the display off.
14. **CH Erase, CH Save buttons**: Press to erase or save channel.
15. **C/C**: Press to select the Closed Caption mode.
16. **V-Chip**: Press to select the child protect mode.
17. **Number buttons**: Press 0~9,100 to select a channel; the channel changes after 2 seconds.
18. **PIP Source**: Press to select the signal for Sub Window.(Only for PIP.)
19. **F.WHITE**: Press to show a full white picture.
20. **PREV**: Press it returns to the last viewed channel.(Only for TV.)

(Continued on next page)

21 **SOUND**: Press to select different sound system, such as Normal, Flat, News, Cinema, User or BBE Digital.
22 **PICTURE**: Press to select "BRIGHTNESS", "COLOR", "CONTRAST", "HUE" or "SHARPNESS", and you can use ◀ or ▶ to adjust.
23 **EXIT**: Press to return or exit OSD menu.
24 **SOURCE**: Press to select the signal sources directly. Such as TV, AV1, S-VIDEO, YCbCr, YPbPr, Analog RGB or Digital RGB.
25 **MENU**: Press to display the OSD Menu.
26 **OK**: Press to enter or confirm.
27 ▲ / ▼: They are used as ▲ / ▼ buttons in the OSD Menu screen and they can be used for the selection of the program when the OSD Menu is not shown on the screen.
28 ◀ / ▶: They are used as ◀ / ▶ buttons in the OSD Menu screen and they can be used for the adjustment of volume when the OSD Menu is not shown on the screen.

PHYSICAL CHARACTERISTICS

14. Power Cord

Length : 1.8m nominal

Type : optional

15. Cabinet

15.1 Color : silver colour as defined by colour plaque reference number

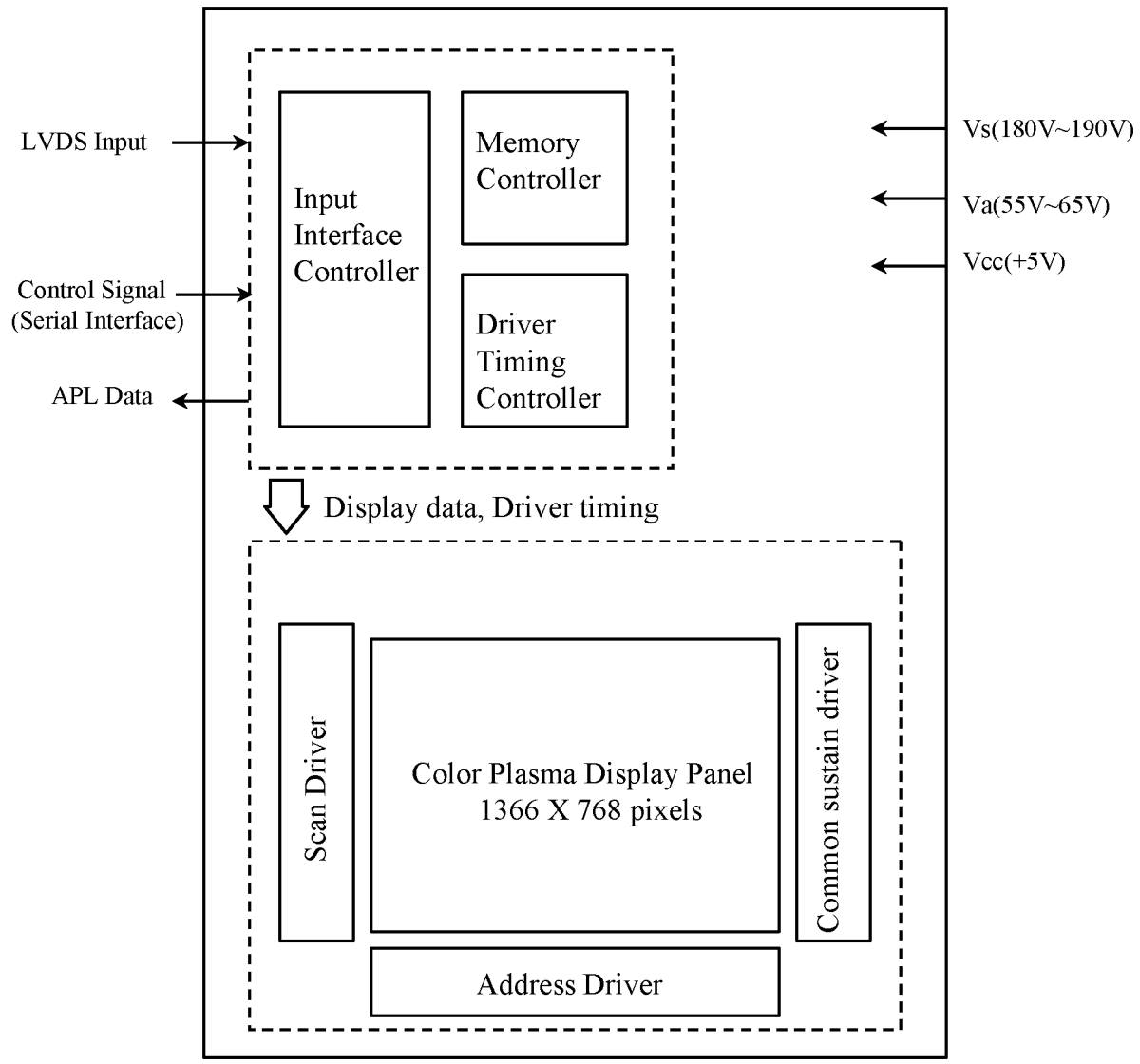
15.2 Weight

Net weight : 51.8kg
Gross weight : 74kg

15.3 Dimensions (w/o stand&handles)

Width : 1227.8mm
Height : 739.8mm
Depth : 122.7mm

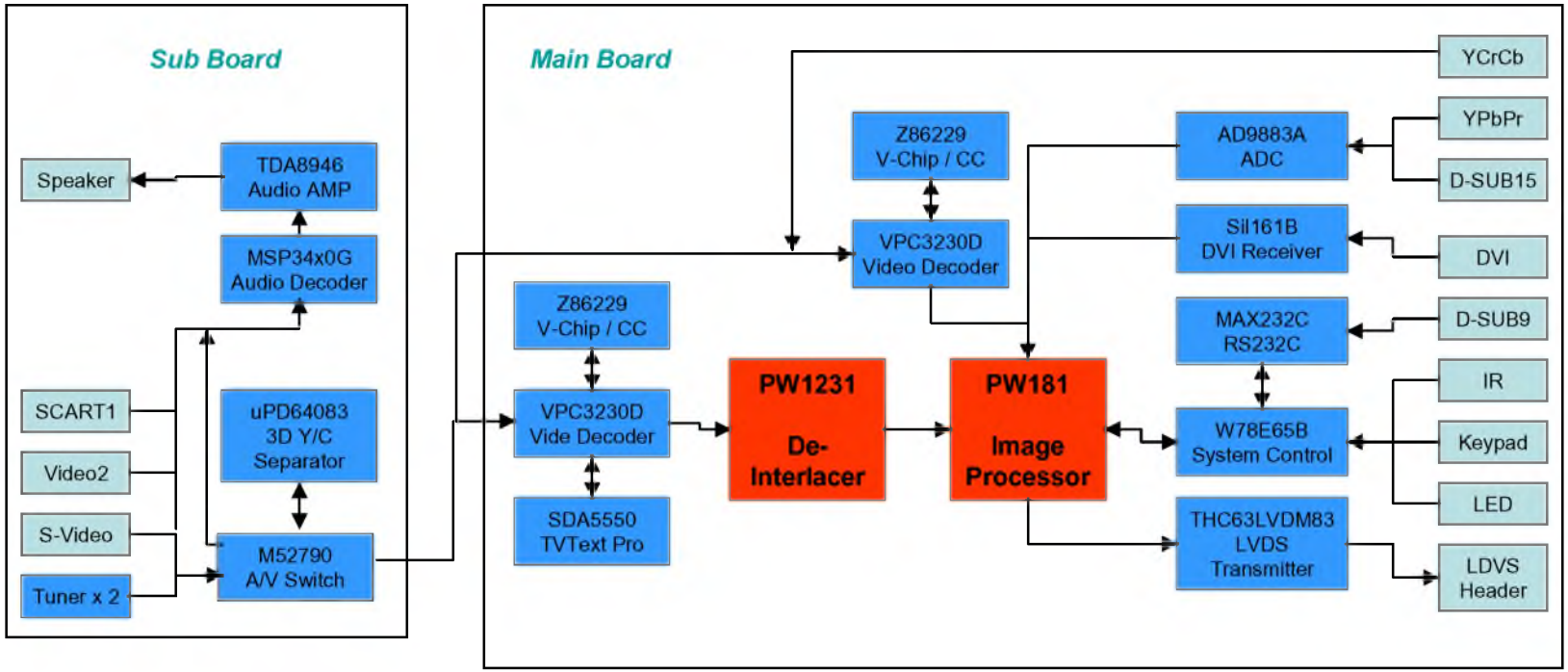
Block Diagram



☞ Applied Voltage level is specified at the time when Full-White pattern is displayed on the panel.

Block Diagram

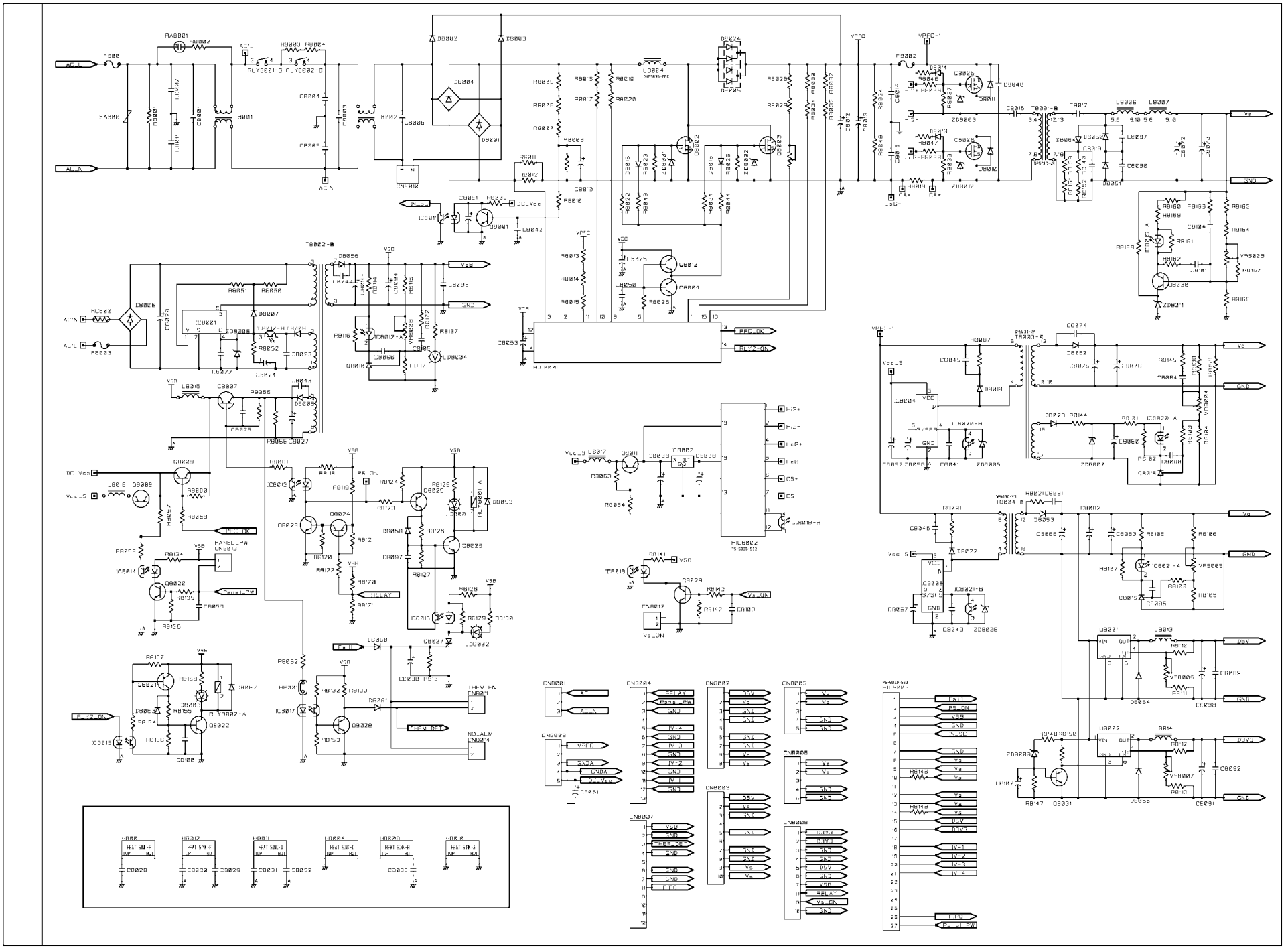
MAIN/AUDIO BOARD

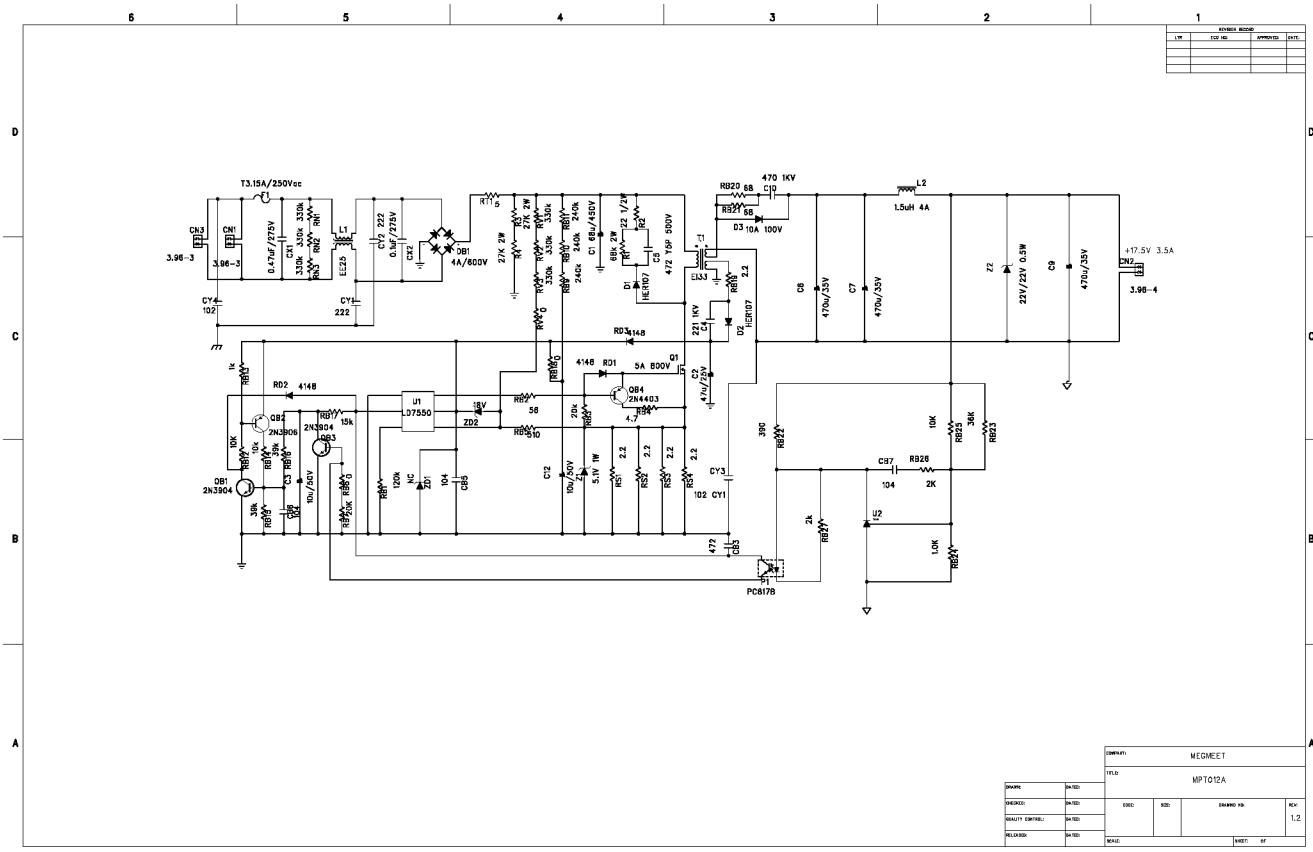


Circuit Diagram

- Power supply board of Audio Amplifier,
- Main (Video) board
- Audio/Tuner board
- Keypad board
- Remote control receiver board
- Remote control board

MPT012A

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F1
CN2
3.96-3
CN1
3.96-3
0.47nF/275V
CX1
330k
RR1
330k
RR2
L1
EE25
CY2 222
0.1uF/275V
CX2
DB1
4A/600V
RT1 5
27K 2W
R4
27K 2W
R3
330k
RR7
330k
RR6
240k
RR5
240k
RR4
330k
RR3
C1 68u/450V
68K 2W
R1
22 1/2W
R2
C5
472 1KV 500V
T1
EE33
D1
HER107
RR10
2.2
CY4
102
CY1
222
RR9
4.7
221 1KV
C4
D2
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RR8
0
RR11
0
4148
RD1
Q1
5A 800V
C2
470u/25V
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RR14
4.7
U1
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18V
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RB9
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DB1
2N3904
RR20
39k
RR21
20K
C3
RR22
120k
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C12
10u/50V
5.1V 1W
RR24
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RR25
2.2
RR26
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RR27
2.2
CY3
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CB3
PC817B
RB20 6R
C10
470 1KV
RB21 6R
D3 10A 100V
L2
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C8
470u/35V
C7
470u/35V
Z2
22V/22V 0.5W
C9
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+17.5V 3.5A
CN3
3.96-4
RR22
390
RR23
10K
RR24
36K
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C87
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RR26
2K
L2
RR27
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LOK
RR28
REVISION RECORD
LTR
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APPROVED
DATE
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MEGMEET
TITLE:
MPT012A
DRAWN:
DATE:
CHECKED:
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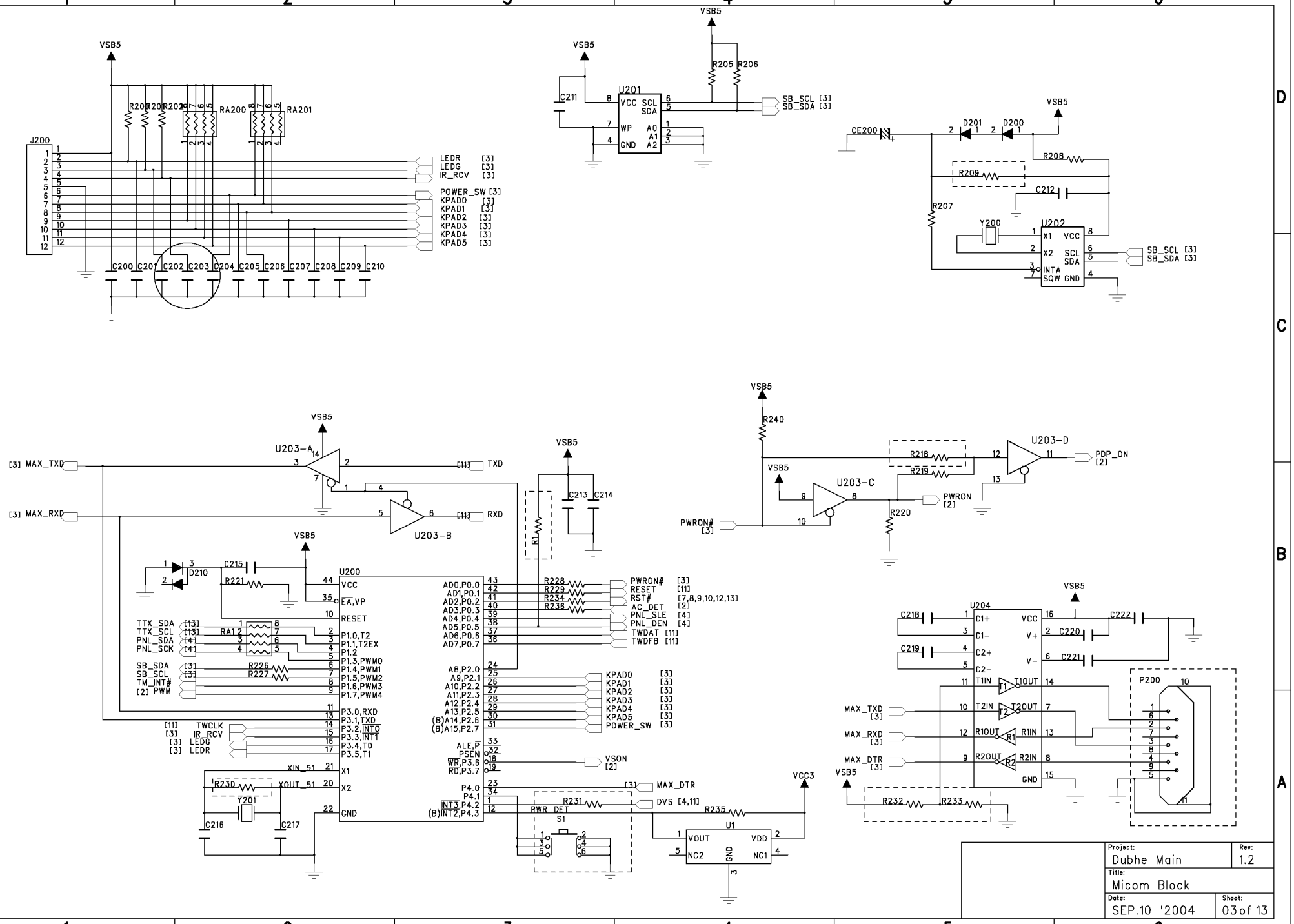
RELEASED:
DCO:
SIZE:
DRAWING NO.
REV:
1.2
SCALE:
SHEET: OF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RA201
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U203-B
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U203-D
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Y201
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Rev: 1.2
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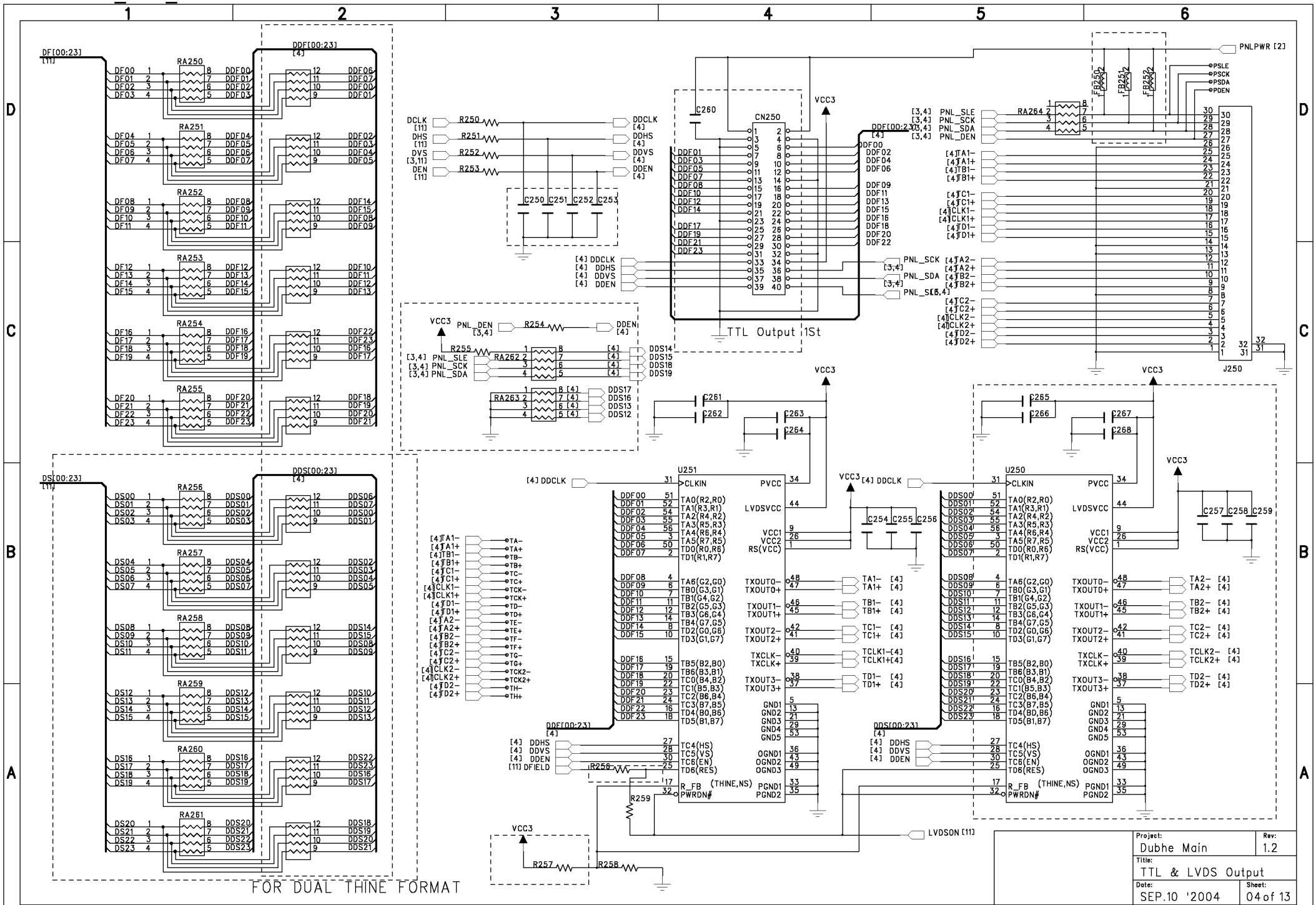
Date: SEP.10 '2004
Sheet: 03of 13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RA253
RA254
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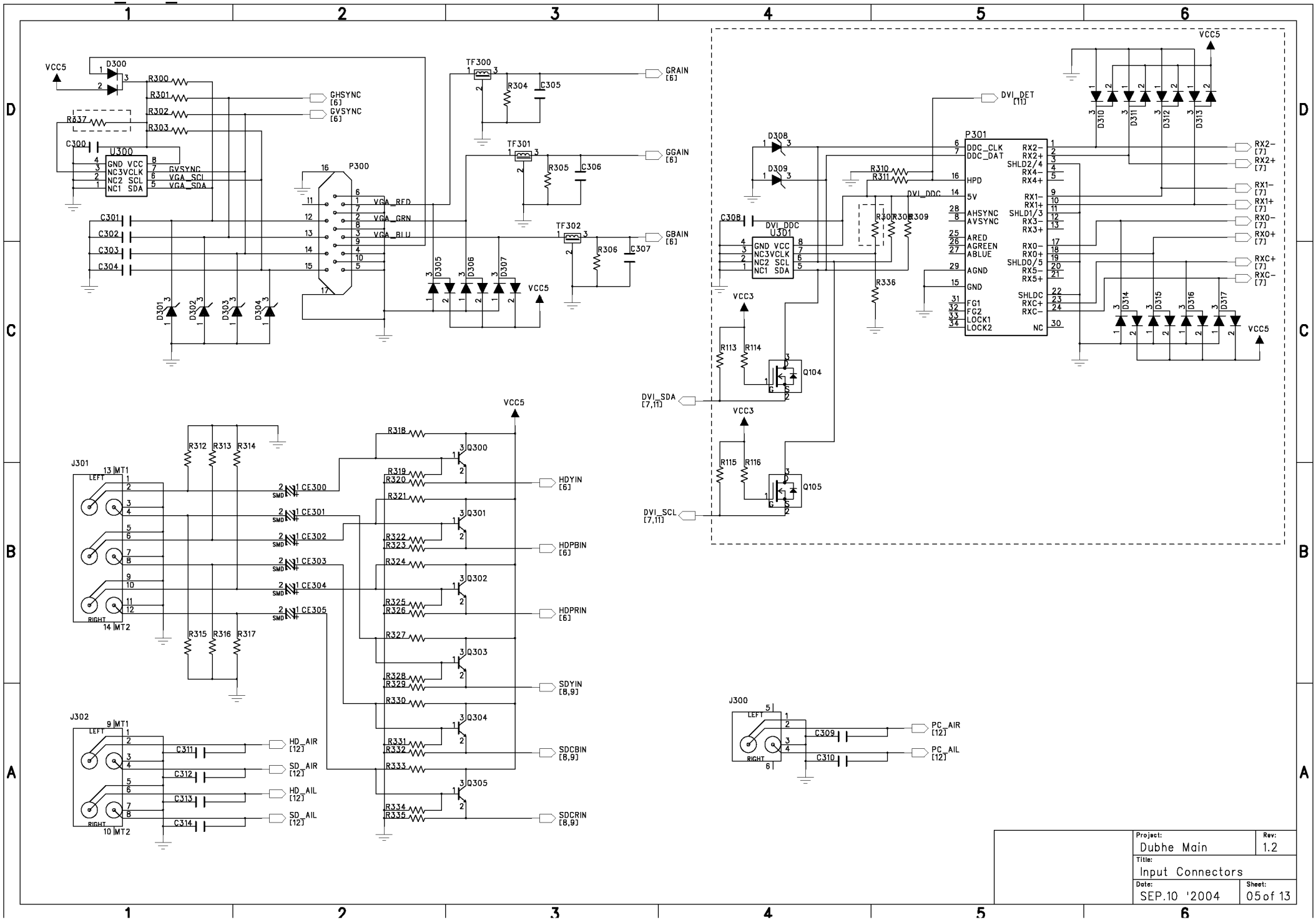
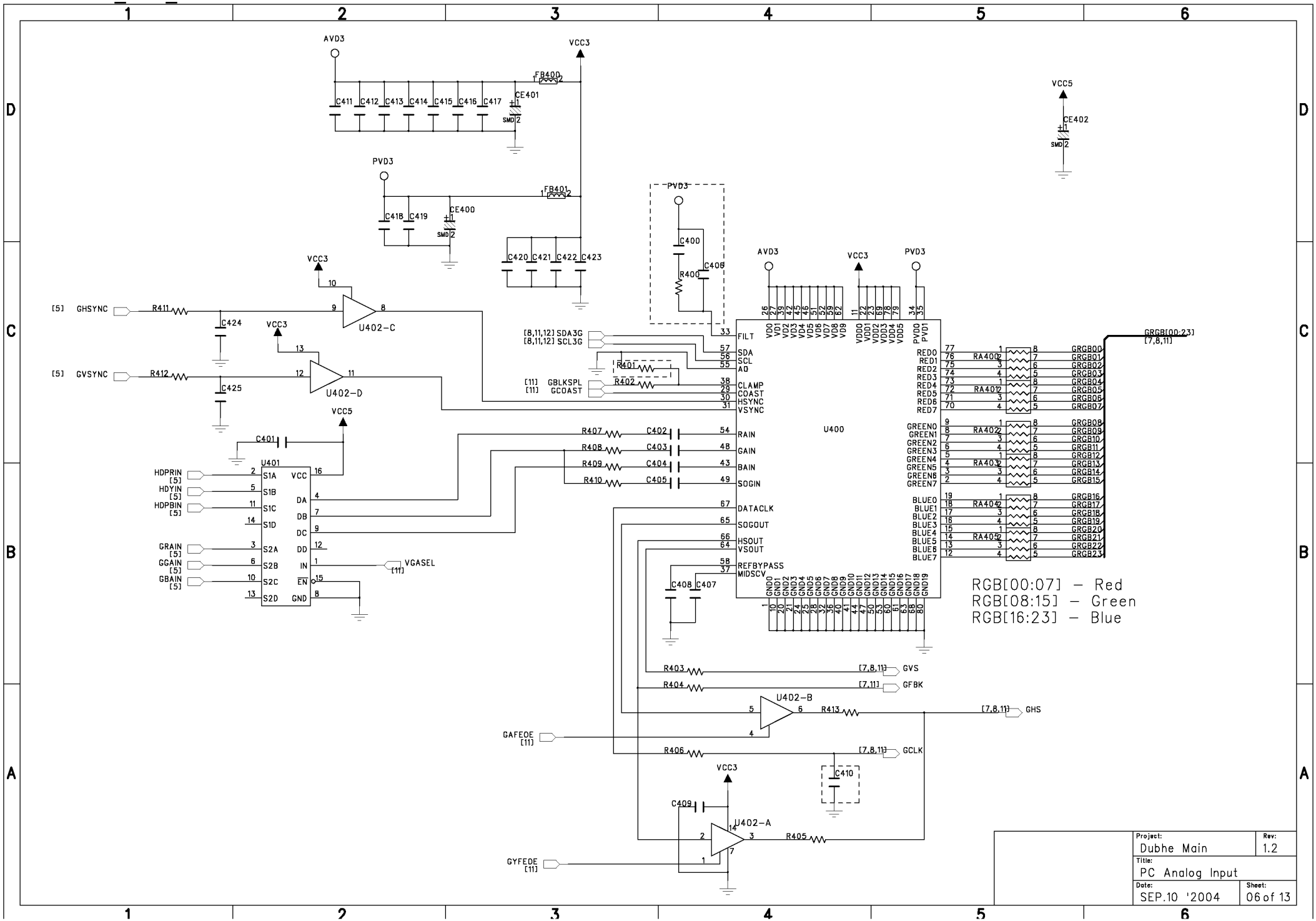
R250
R251
R252
R253
DCLK
DHS
DVS
DEN
DDCLK
DDHS
DDVS
DDEN
TTL Output 1St
PNLPWR [2]
PSLE
PSCK
PSDA
PDEN
PNL_SLE
PNL_SCK
PNL_SDA
PNL_DEN
RA264
J250
R254
R255
RA262
RA263
DDS14
DDS15
DDS18
DDS19
DDS17
DDS16
DDS13
DDS12
C261
C262
C263
C264
C265
C266
C267
C268
C254 C255 C256
C257 C258 C259
U251
U250
CLKIN
PVCC
LVDSVCC
VCC1
VCC2
RS(VCC)
TXOUT0-
TXOUT0+
TXOUT1-
TXOUT1+
TXOUT2-
TXOUT2+
TXCLK-
TXCLK+
TXOUT3-
TXOUT3+
GND1
GND2
GND3
GND4
GND5
OGND1
OGND2
OGND3
PGND1
PGND2
R_FB
PWRDN#
(THINE,NS)
R256
R259
R257
R258
LVDSON [11]
FOR DUAL THINE FORMAT
Project: Dubhe Main
Rev: 1.2
Title: TTL & LVDS Output
Date: SEP.10 '2004
Sheet: 04 of 13


VCC5
D300
R300
R301
R302
R303
R337
C300
U300
GND VCC
NC3VCLK
NC2 SCL
NC1 SDA
GVSYNC
VGA_SCL
VGA_SDA
CHSYNC [6]
GVSYNC [6]
P300
VGA_RED
VGA_GRN
VGA_BLU
C301
C302
C303
C304
D301
D302
D303
D304
TF300
TF301
TF302
R304
R305
R306
C305
C306
C307
GRAIN [6]
GGAIN [6]
GBAIN [6]
D305
D306
D307
DVI_DET [11]
P301
DDC_CLK
DDC_DAT
HPD
5V
AHSYNC
AVSYNC
ARED
AGREEN
ABLUE
AGND
GND
FG1
FG2
LOCK1
LOCK2
RX2-
RX2+
SHLD2/4
RX4-
RX4+
RX1-
RX1+
SHLD1/3
RX3-
RX3+
RX0-
RX0+
SHLDO/5
RX5-
RX5+
SHLDC
RXC+
RXC-
NC
D308
D309
D310
D311
D312
D313
D314
D315
D316
D317
R310
R311
R308
R309
R336
C308
U301
DVI_DDC
VCC3
R113
R114
R115
R116
Q104
Q105
DVI_SDA [7,11]
DVI_SCL [7,11]
J301
13 MT1
14 MT2
LEFT
RIGHT
R312
R313
R314
R315
R316
R317
CE300
CE301
CE302
CE303
CE304
CE305
R318
R319
R320
R321
R322
R323
R324
R325
R326
R327
R328
R329
R330
R331
R332
R333
R334
R335
Q300
Q301
Q302
Q303
Q304
Q305
HDYIN [6]
HDPBIN [6]
HDPRIN [6]
SDYIN [8,9]
SDCBIN [8,9]
SDCRIN [8,9]
J302
9 MT1
10 MT2
C311
C312
C313
C314
HD_AIR [12]
SD_AIR [12]
HD_AIL [12]
SD_AIL [12]
J300
C309
C310
PC_AIR [12]
PC_AIL [12]
Project: Dubhe Main
Rev: 1.2
Title: Input Connectors
Date: SEP.10 '2004
Sheet: 05of 13


AVD3
VCC3
VCC5
PVD3
FB400
FB401
C411 C412 C413 C414 C415 C416 C417
CE401
C418 C419
CE400
C420 C421 C422 C423
CE402
C400
C406
R400
[5] GHSYNC
R411
C424
U402-C
[5] GVSYNC
R412
C425
U402-D
[8,11,12] SDA3G
[8,11,12] SCL3G
R401
R402
[11] GBLKSPL
[11] GCOAST
U400
FILT
SDA
SCL
A0
CLAMP
COAST
HSYNC
VSYNC
RAIN
GAIN
BAIN
SOGIN
DATACLK
SOGOUT
HSOUT
VSOUT
REFBYPASS
MIDSCV
REDO
RED1
RED2
RED3
RED4
RED5
RED6
RED7
GREEN0
GREEN1
GREEN2
GREEN3
GREEN4
GREEN5
GREEN6
GREEN7
BLUE0
BLUE1
BLUE2
BLUE3
BLUE4
BLUE5
BLUE6
BLUE7
RA400
RA401
RA402
RA403
RA404
RA405
GRGB[00:23]
[7,8,11]
R407 C402
R408 C403
R409 C404
R410 C405
C408 C407
U401
S1A
S1B
S1C
S1D
S2A
S2B
S2C
S2D
VCC
GND
DA
DB
DC
DD
IN
EN
HDPRIN [5]
HDYIN [5]
HDPBIN [5]
GRAIN [5]
GGAIN [5]
GBAIN [5]
VGASEL [11]
R403 [7,8,11] GVS
R404 [7,11] GFBK
U402-B
R413 [7,8,11] GHS
GAFEOE [11]
R406 [7,8,11] GCLK
C410
C409
U402-A
R405
GYFEDE [11]
RGB[00:07] - Red
RGB[08:15] - Green
RGB[16:23] - Blue
Project: Dubhe Main
Rev: 1.2
Title: PC Analog Input
Date: SEP.10 '2004
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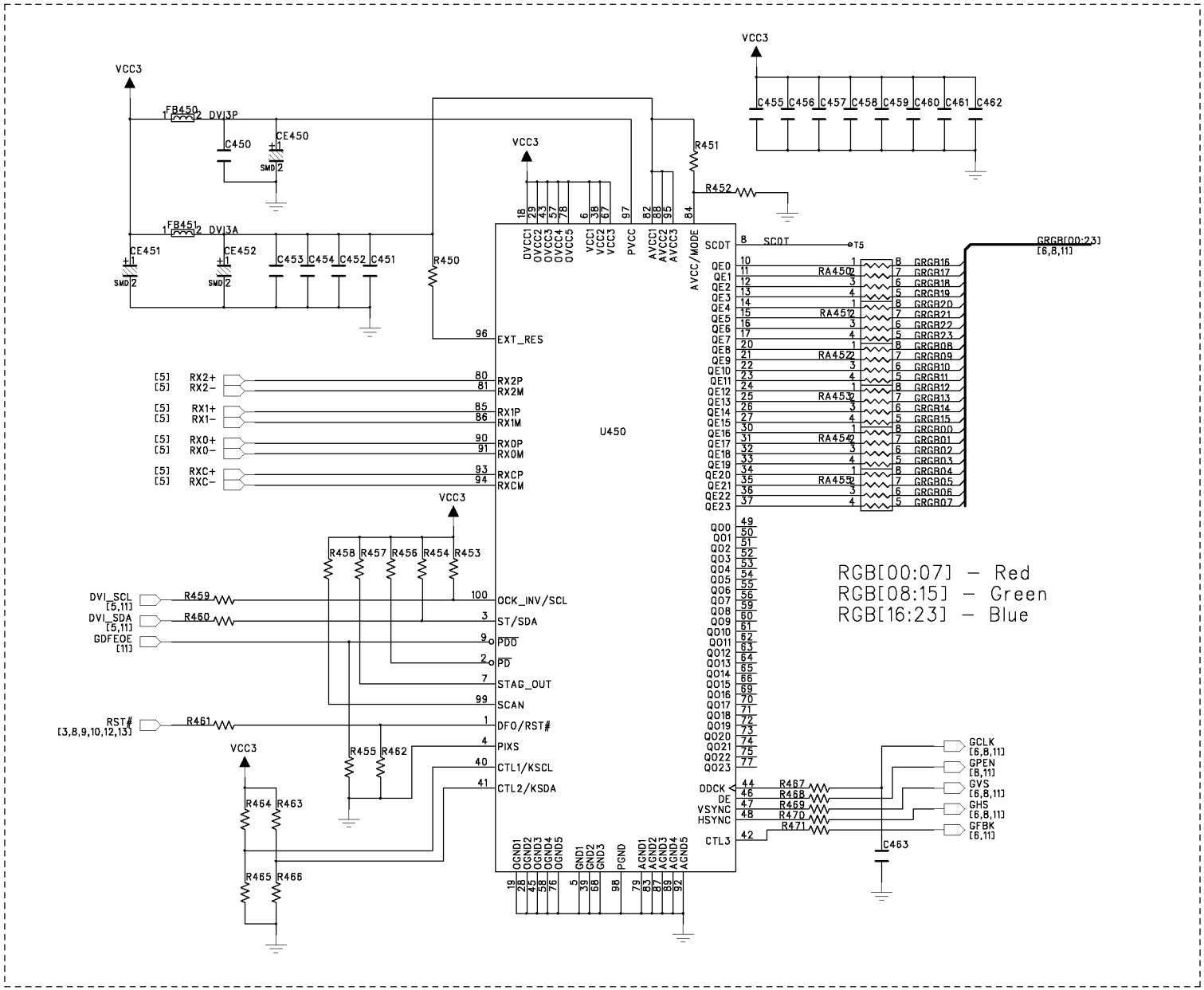
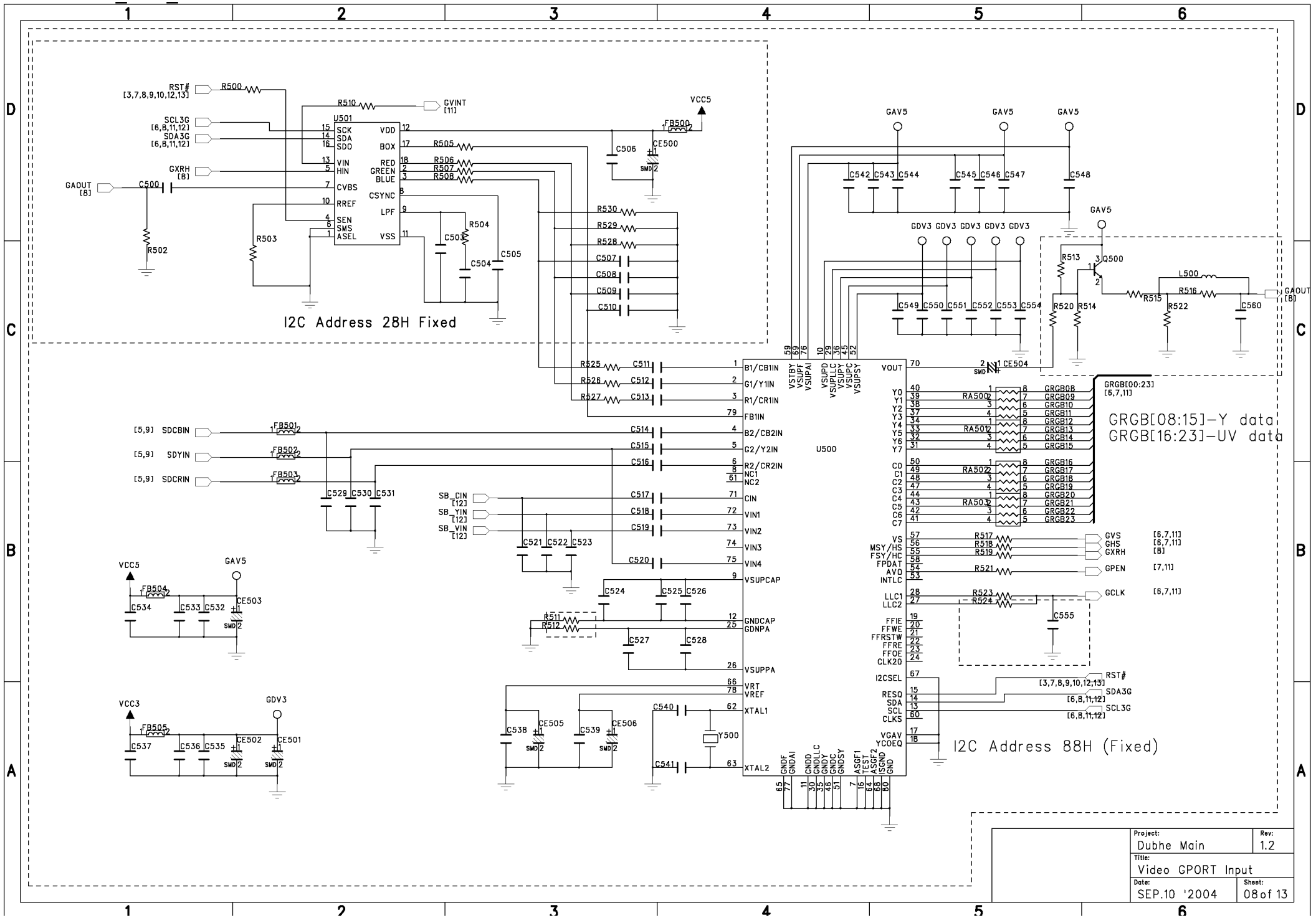
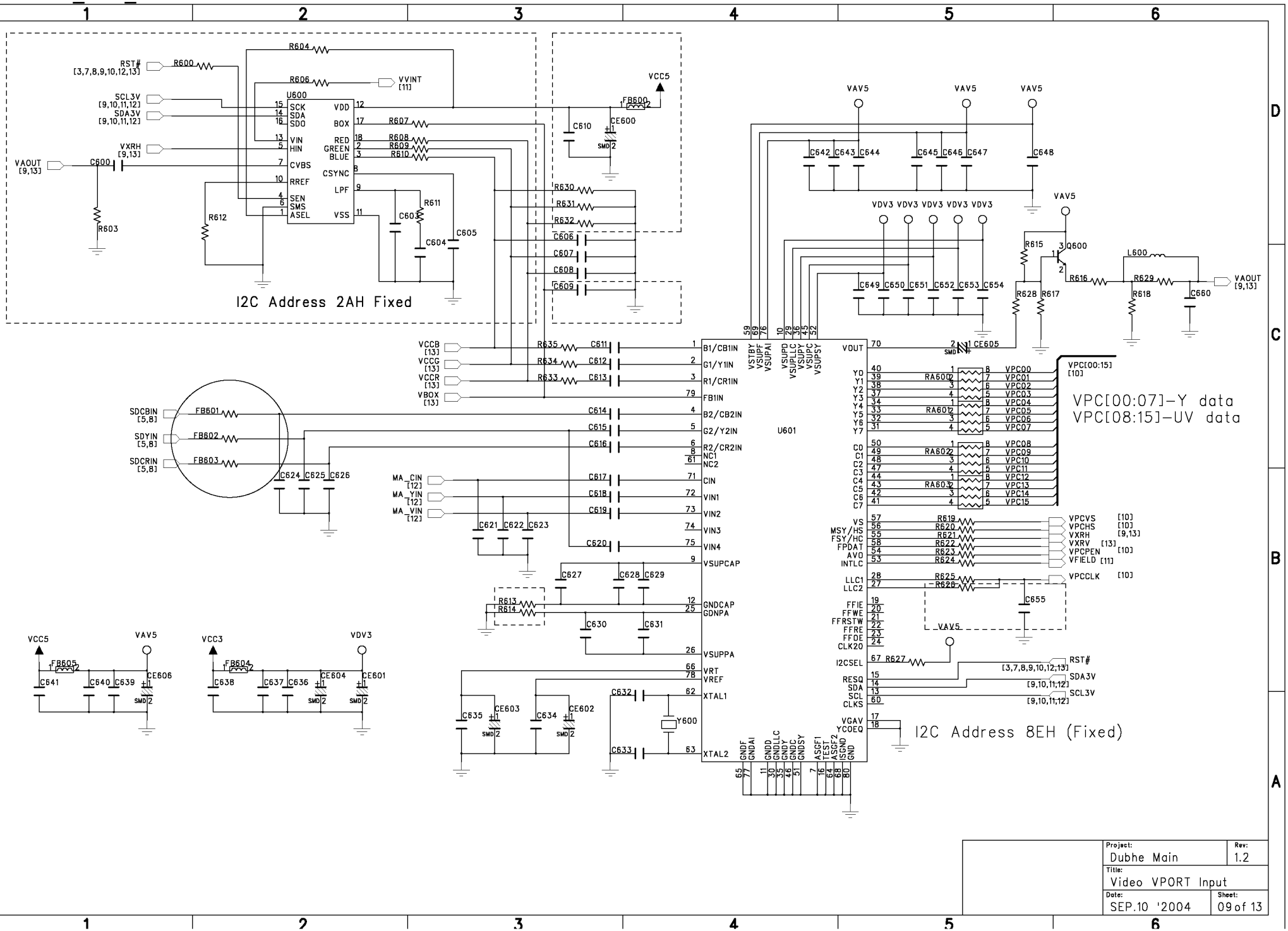


	Project: Dubhe Main	Rev: 1.2
	Title: PC Digital Input	
	Date: SEP.10 '2004	Sheet: 07 of 13


I2C Address 28H Fixed
I2C Address 88H (Fixed)
U500
U501
GRGB[08:15]-Y data
GRGB[16:23]-UV data
Project: Dubhe Main
Rev: 1.2
Title: Video GPORT Input
Date: SEP.10 '2004
Sheet: 08of 13


I2C Address 2AH Fixed
I2C Address 8EH (Fixed)
U600
U601
VPC[00:07]-Y data
VPC[08:15]-UV data
Project: Dubhe Main
Rev: 1.2
Title: Video VPORT Input
Date: SEP.10 '2004
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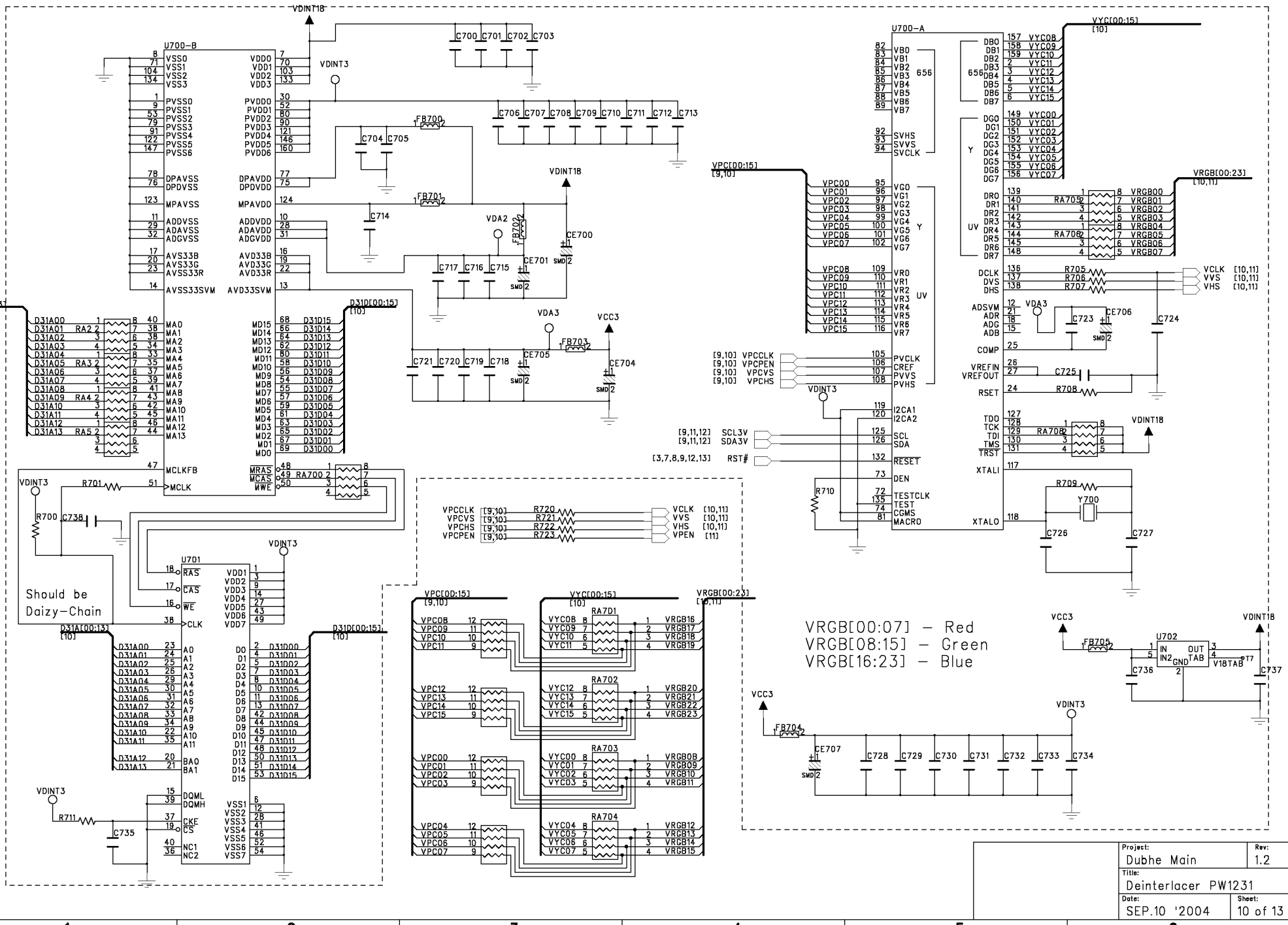
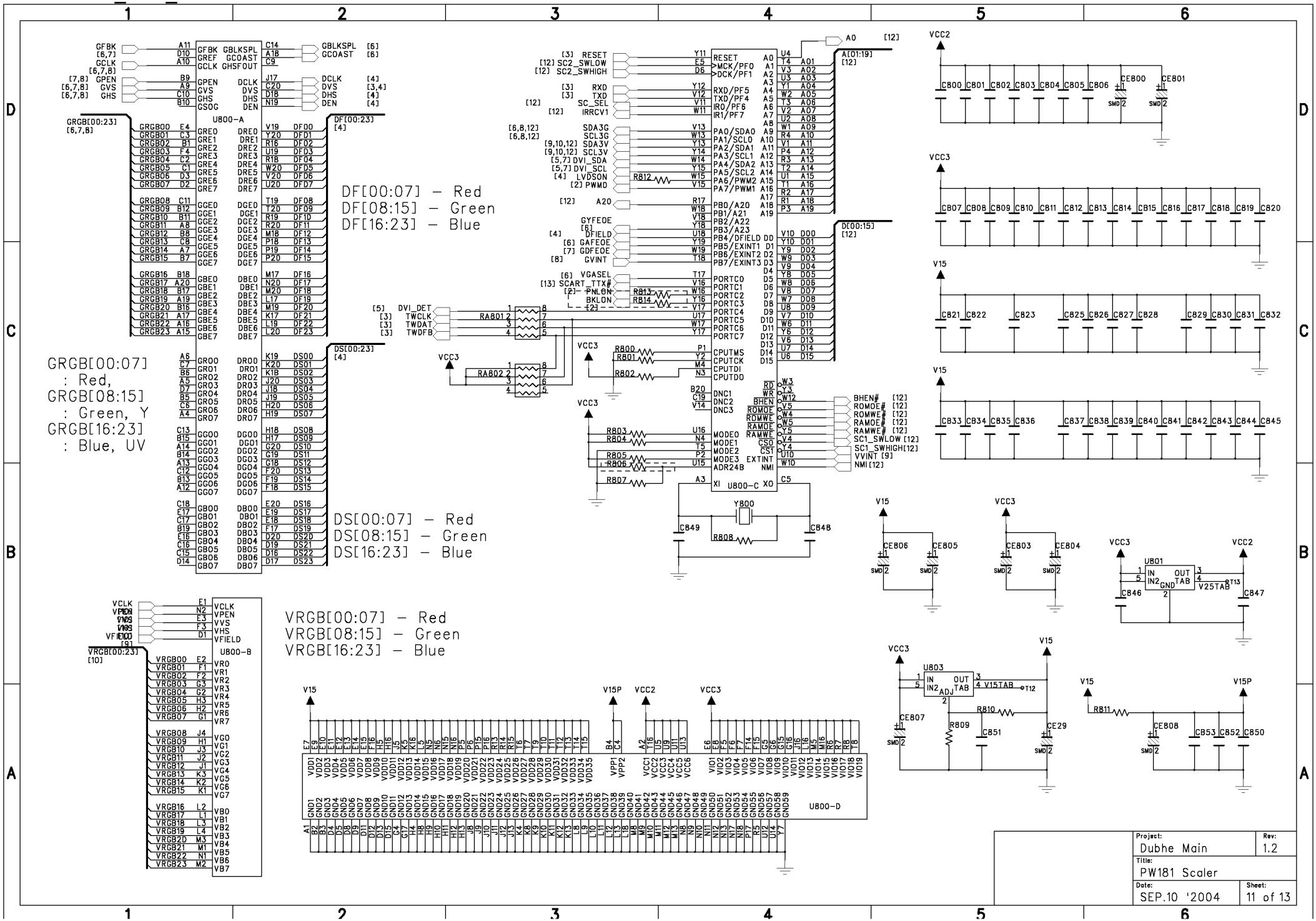
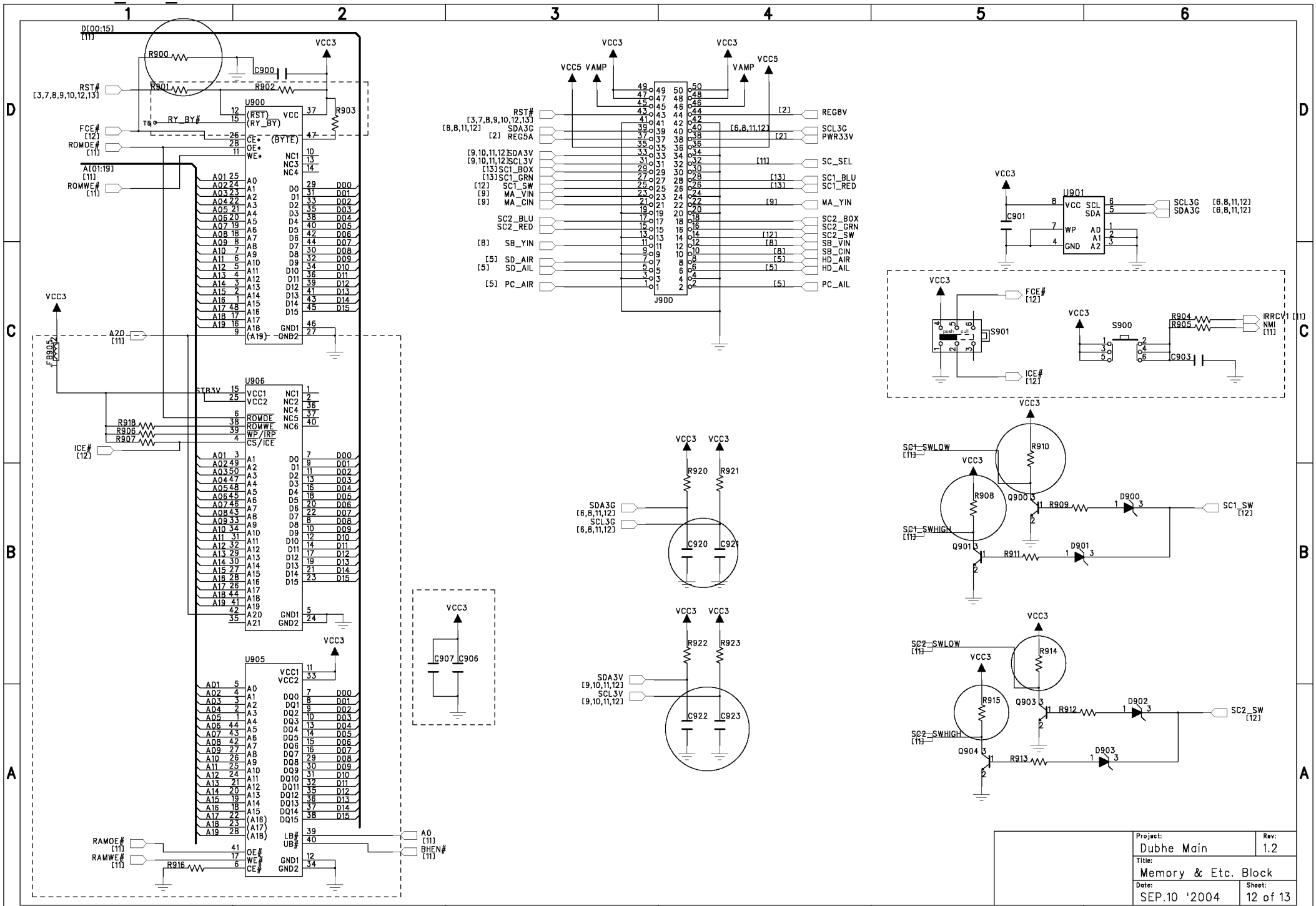

U700-B
U700-A
U701
Should be
Daizy-Chain
VRGB[00:07] - Red
VRGB[08:15] - Green
VRGB[16:23] - Blue
Project: Dubhe Main
Rev: 1.2
Title: Deinterlacer PW1231
Date: SEP.10 '2004
Sheet: 10 of 13


GRGB[00:07] : Red, GRGB[08:15] : Green, Y GRGB[16:23] : Blue, UV
DF[00:07] – Red
DF[08:15] – Green
DF[16:23] – Blue
DS[00:07] – Red
DS[08:15] – Green
DS[16:23] – Blue
VRGB[00:07] – Red
VRGB[08:15] – Green
VRGB[16:23] – Blue
U800-A
U800-B
U800-C
U800-D
Y800
U801
U803
Project: Dubhe Main
Rev: 1.2
Title: PW181 Scaler
Date: SEP.10 '2004
Sheet: 11 of 13


D[00:15]
[11]
R900
C900
VCC3
RST#
[3,7,8,9,10,12,13]
R901
R902
R903
U900
RY_BY#
FCE#
[12]
ROMOE#
[11]
ROMWE#
[11]
A[01:19]
[11]
A20
[11]
FB905
U906
R918
R906
R907
ICE#
[12]
U905
RAMOE#
[11]
RAMWE#
[11]
R916
A0
[11]
BHEN#
[11]
C907 C906
J900
REGBV
SCL3G
PWR33V
SC_SEL
SC1_BLU
SC1_RED
MA_YIN
SC2_BOX
SC2_GRN
SC2_SW
SB_VIN
SB_CIN
HD_AIR
HD_AIL
PC_AIL
R920
R921
C920
C921
R922
R923
C922
C923
U901
C901
S901
S900
R904
R905
IRRCV1 [11]
NMI [11]
C903
R910
R908
Q900
R909
D900
SC1_SW
[12]
SC1_SWLOW
[11]
SC1_SWHIGH
[11]
Q901
R911
D901
R914
R915
Q903
R912
D902
SC2_SW
[12]
SC2_SWLOW
[11]
SC2_SWHIGH
[11]
Q904
R913
D903
Project:
Dubhe Main
Rev:
1.2
Title:
Memory & Etc. Block
Date:
SEP.10 '2004
Sheet:
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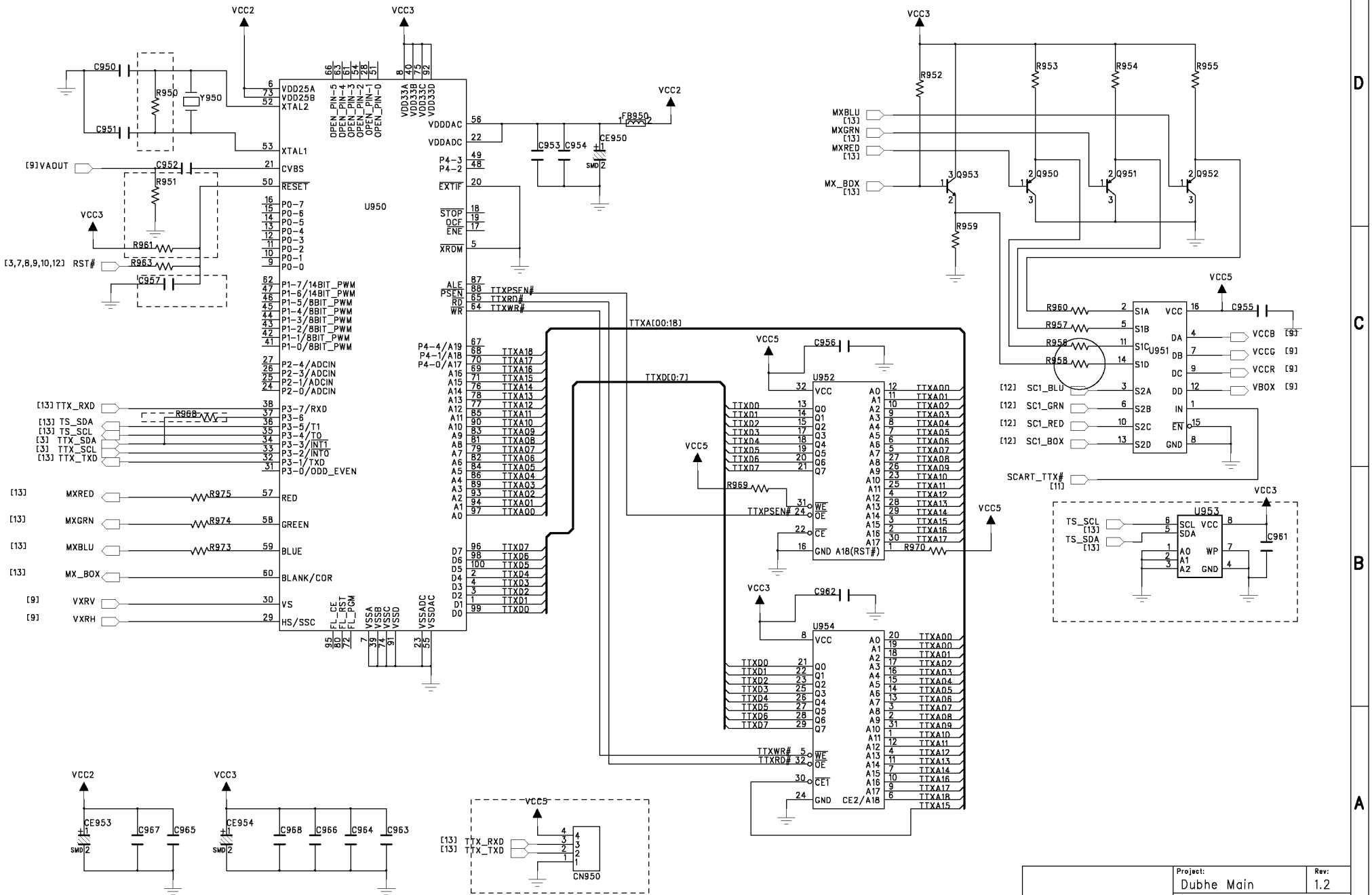
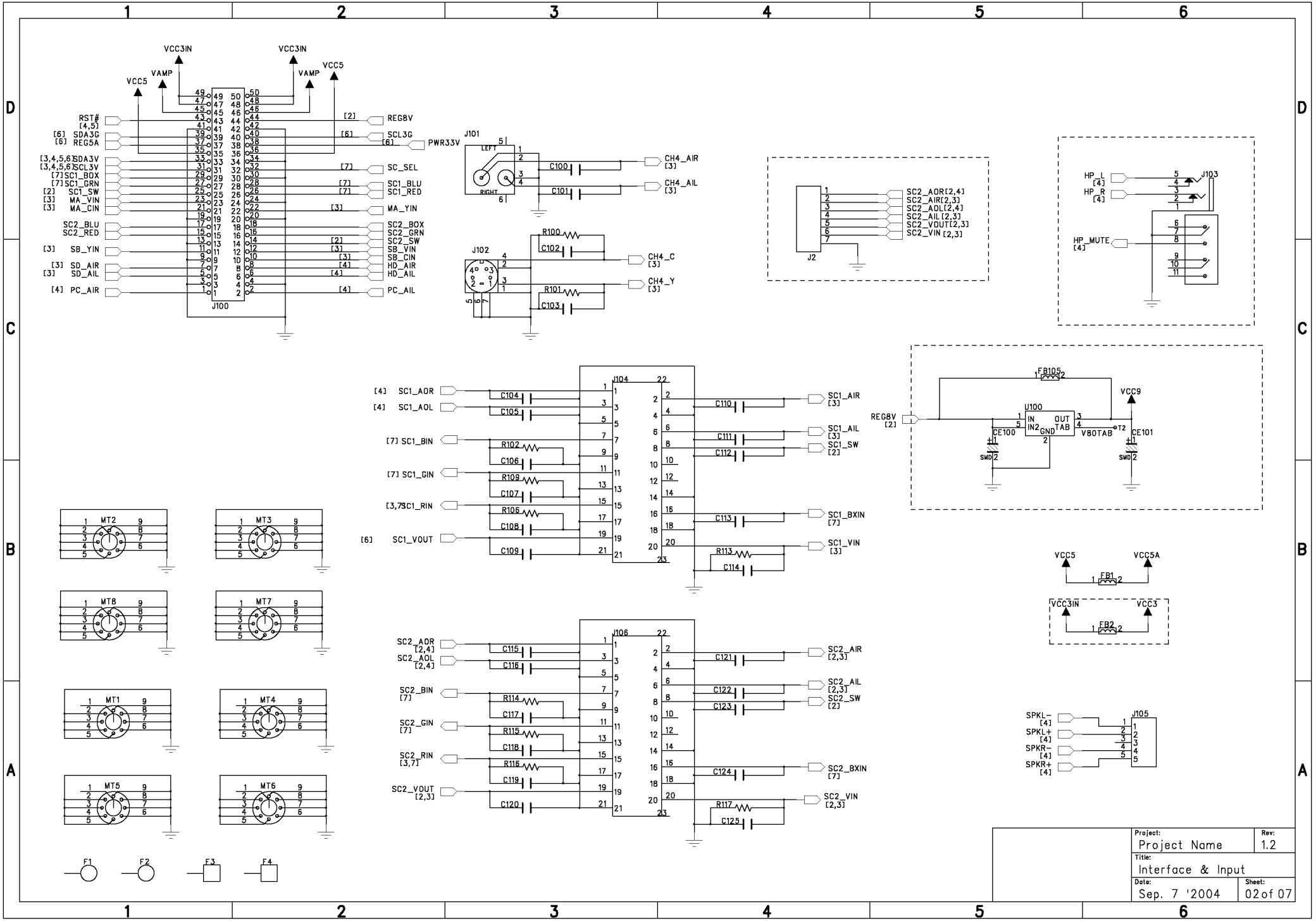

U950
U951
U952
U953
U954
CN950
TTXA[00:18]
TTXD[0:7]
Project: Dubhe Main
Rev: 1.2
Title: TTX Processor
Date: SEP.10 '2004
Sheet: 13 of 13


VCC3IN
VCC5
VAMP
J100
J101
J102
J103
J104
J105
J106
J2
RST#
REG8V
SDA3G
SCL3G
REG5A
PWR33V
SDA3V
SCL3V
SC_SEL
SC1_BOX
SC1_GRN
SC1_SW
SC1_MA_VIN
SC1_MA_CIN
SC1_BLU
SC1_RED
MA_YIN
SC2_BLU
SC2_RED
SC2_BOX
SC2_GRN
SC2_SW
SB_YIN
SB_VIN
SB_CIN
SD_AIR
SD_AIL
HD_AIR
HD_AIL
PC_AIR
PC_AIL
CH4_AIR
CH4_AIL
CH4_C
CH4_Y
SC2_AOR[2,4]
SC2_AIR[2,3]
SC2_AOL[2,4]
SC2_AIL[2,3]
SC2_VOUT[2,3]
SC2_VIN[2,3]
HP_L
HP_R
HP_MUTE
SC1_AOR
SC1_AOL
SC1_BIN
SC1_GIN
SC1_RIN
SC1_VOUT
SC1_AIR
SC1_AIL
SC1_SW
SC1_BXIN
SC1_VIN
SC2_AOR
SC2_AOL
SC2_BIN
SC2_GIN
SC2_RIN
SC2_VOUT
SC2_AIR
SC2_AIL
SC2_SW
SC2_BXIN
SC2_VIN
FB105
VCC9
U100
IN
IN2
GND
OUT
TAB
V80TAB
CE100
CE101
VCC5A
FB1
VCC3
FB2
SPKL-
SPKL+
SPKR-
SPKR+
MT1
MT2
MT3
MT4
MT5
MT6
MT7
MT8
F1
F2
F3
F4
Project:
Project Name
Rev:
1.2
Title:
Interface & Input
Date:
Sep. 7 '2004
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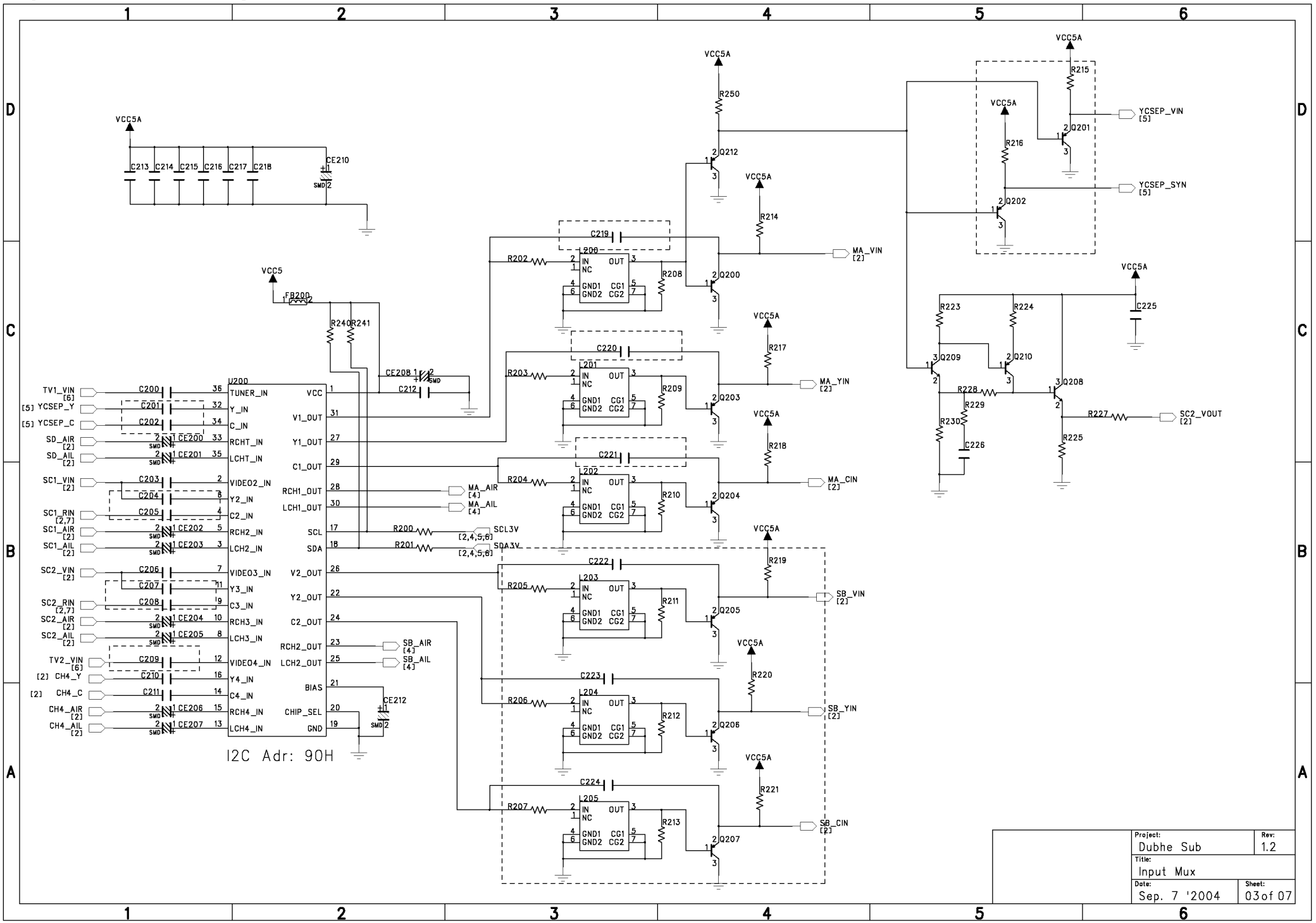
U200
TUNER_IN
Y_IN
C_IN
RCHT_IN
LCHT_IN
VIDEO2_IN
Y2_IN
C2_IN
RCH2_IN
LCH2_IN
VIDEO3_IN
Y3_IN
C3_IN
RCH3_IN
LCH3_IN
VIDEO4_IN
Y4_IN
C4_IN
RCH4_IN
LCH4_IN
VCC
V1_OUT
Y1_OUT
C1_OUT
RCH1_OUT
LCH1_OUT
SCL
SDA
V2_OUT
Y2_OUT
C2_OUT
RCH2_OUT
LCH2_OUT
BIAS
CHIP_SEL
GND
I2C Adr: 90H
VCC5A
VCC5
MA_VIN [2]
MA_YIN [2]
MA_CIN [2]
SB_VIN [2]
SB_YIN [2]
SB_CIN [2]
MA_AIR [4]
MA_AIL [4]
SB_AIR [4]
SB_AIL [4]
SCL3V [2,4,5,6]
SDA3V [2,4,5,6]
YCSEP_VIN [5]
YCSEP_SYN [5]
SC2_VOUT [2]
Project: Dubhe Sub
Rev: 1.2
Title: Input Mux
Date: Sep. 7 '2004
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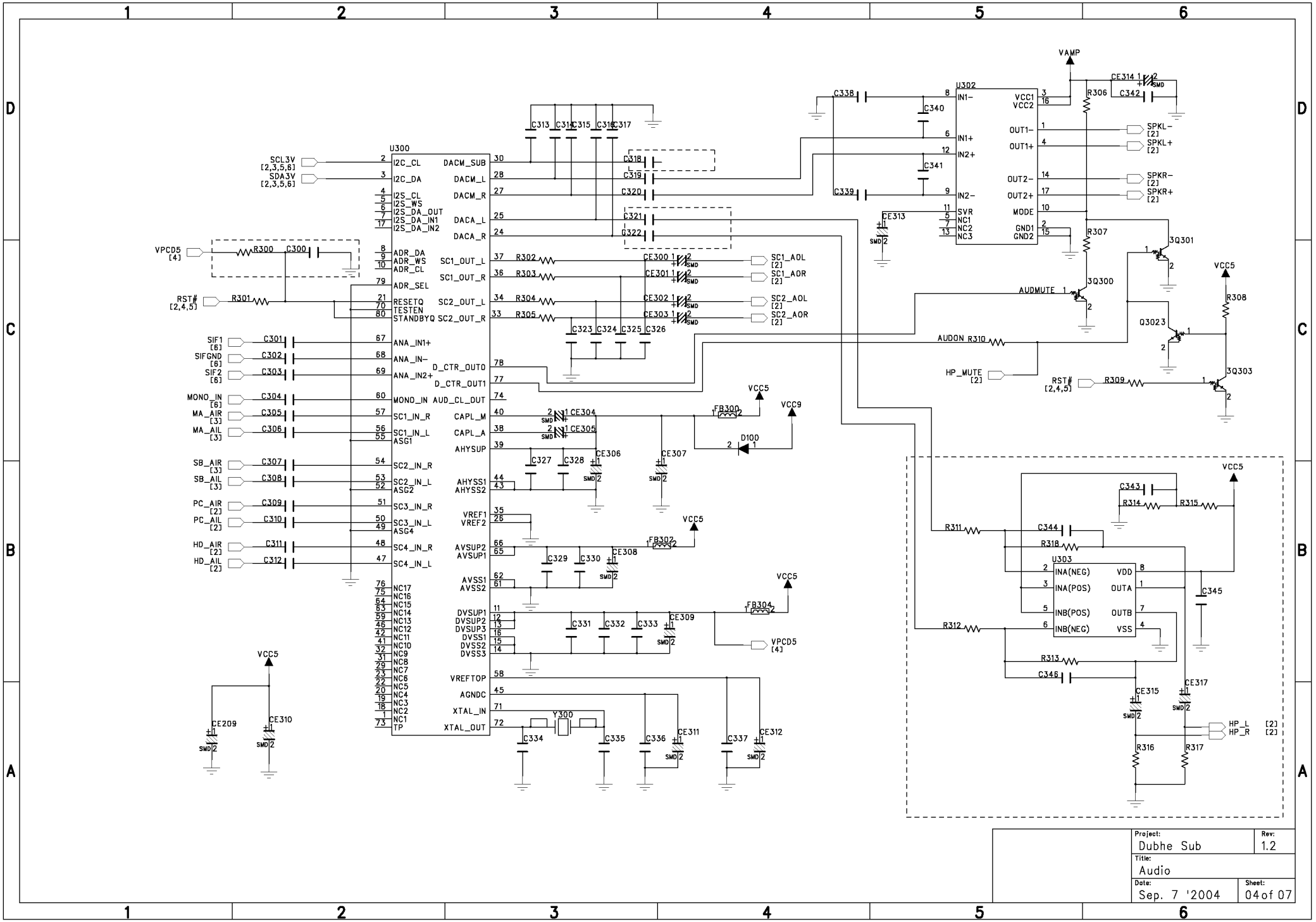
U300
U302
U303
Q3023
3Q300
3Q301
3Q303
D100
VAMP
VCC5
VCC9
VPCD5 [4]
SCL3V [2,3,5,6]
SDA3V [2,3,5,6]
RST# [2,4,5]
SIF1 [6]
SIFGND [6]
SIF2 [6]
MONO_IN [6]
MA_AIR [3]
MA_AIL [3]
SB_AIR [3]
SB_AIL [3]
PC_AIR [2]
PC_AIL [2]
HD_AIR [2]
HD_AIL [2]
SC1_AOL [2]
SC1_AOR [2]
SC2_AOL [2]
SC2_AOR [2]
SPKL- [2]
SPKL+ [2]
SPKR- [2]
SPKR+ [2]
AUDMUTE
AUDON
HP_MUTE [2]
HP_L [2]
HP_R [2]
I2C_CL
I2C_DA
I2S_CL
I2S_WS
I2S_DA_OUT
I2S_DA_IN1
I2S_DA_IN2
ADR_DA
ADR_WS
ADR_CL
ADR_SEL
RESETQ
TESTEN
STANDBYQ
ANA_IN1+
ANA_IN-
ANA_IN2+
MONO_IN
SC1_IN_R
SC1_IN_L
SC2_IN_R
SC2_IN_L
SC3_IN_R
SC3_IN_L
SC4_IN_R
SC4_IN_L
DACM_SUB
DACM_L
DACM_R
DACA_L
DACA_R
SC1_OUT_L
SC1_OUT_R
SC2_OUT_L
SC2_OUT_R
D_CTR_OUT0
D_CTR_OUT1
AUD_CL_OUT
CAPL_M
CAPL_A
AHYSUP
AHYSS1
AHYSS2
VREF1
VREF2
AVSUP2
AVSUP1
AVSS1
AVSS2
DVSUP1
DVSUP2
DVSUP3
DVSS1
DVSS2
DVSS3
VREFTOP
AGNDC
XTAL_IN
XTAL_OUT
IN1-
IN1+
IN2+
IN2-
SVR
MODE
VCC1
VCC2
OUT1-
OUT1+
OUT2-
OUT2+
GND1
GND2
NC1
NC2
NC3
INA(NEG)
INA(POS)
INB(POS)
INB(NEG)
VDD
VSS
OUTA
OUTB
Project: Dubhe Sub
Rev: 1.2
Title: Audio
Date: Sep. 7 '2004
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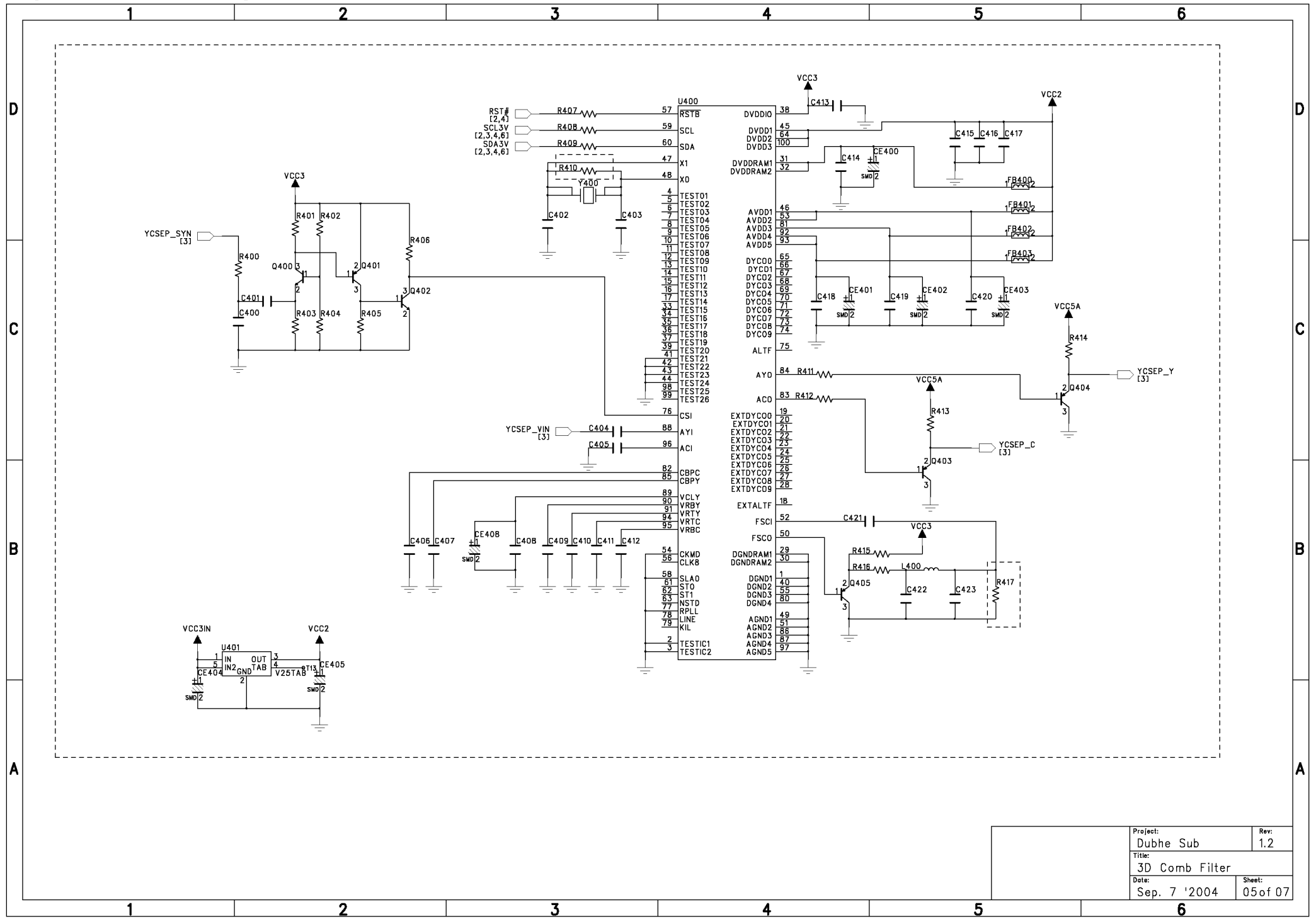
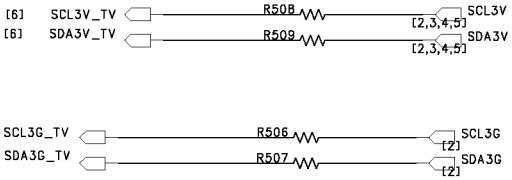
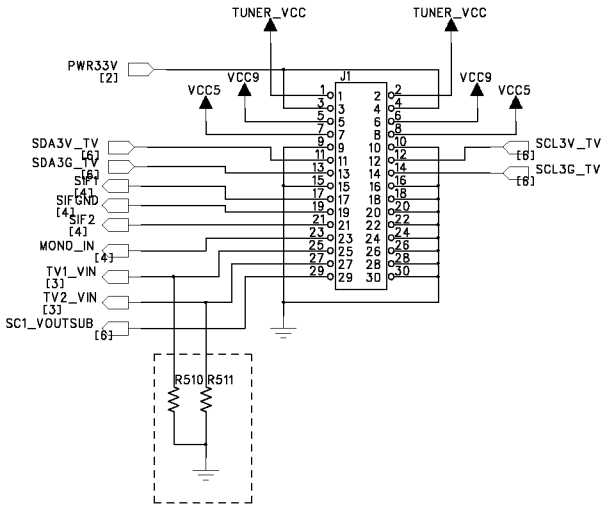
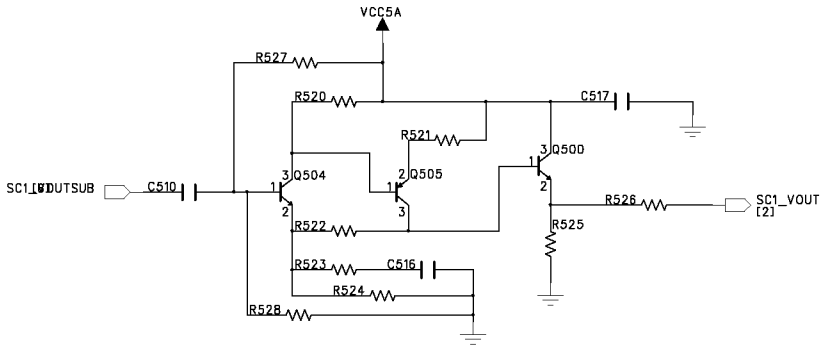
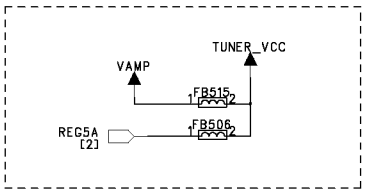


Project: Dubhe Sub	Rev: 1.2
Title: 3D Comb Filter	
Date: Sep. 7 '2004	Sheet: 05of 07

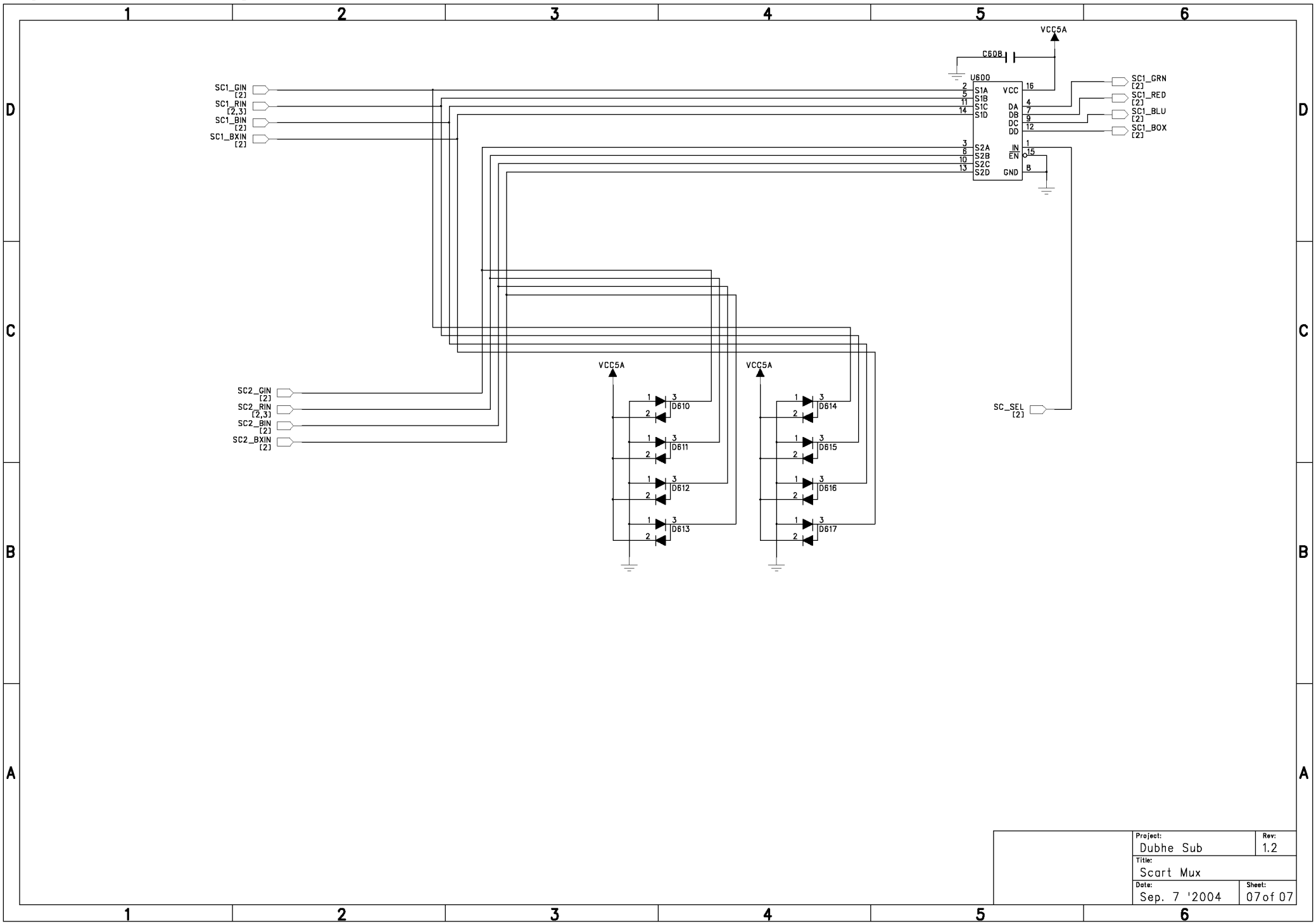


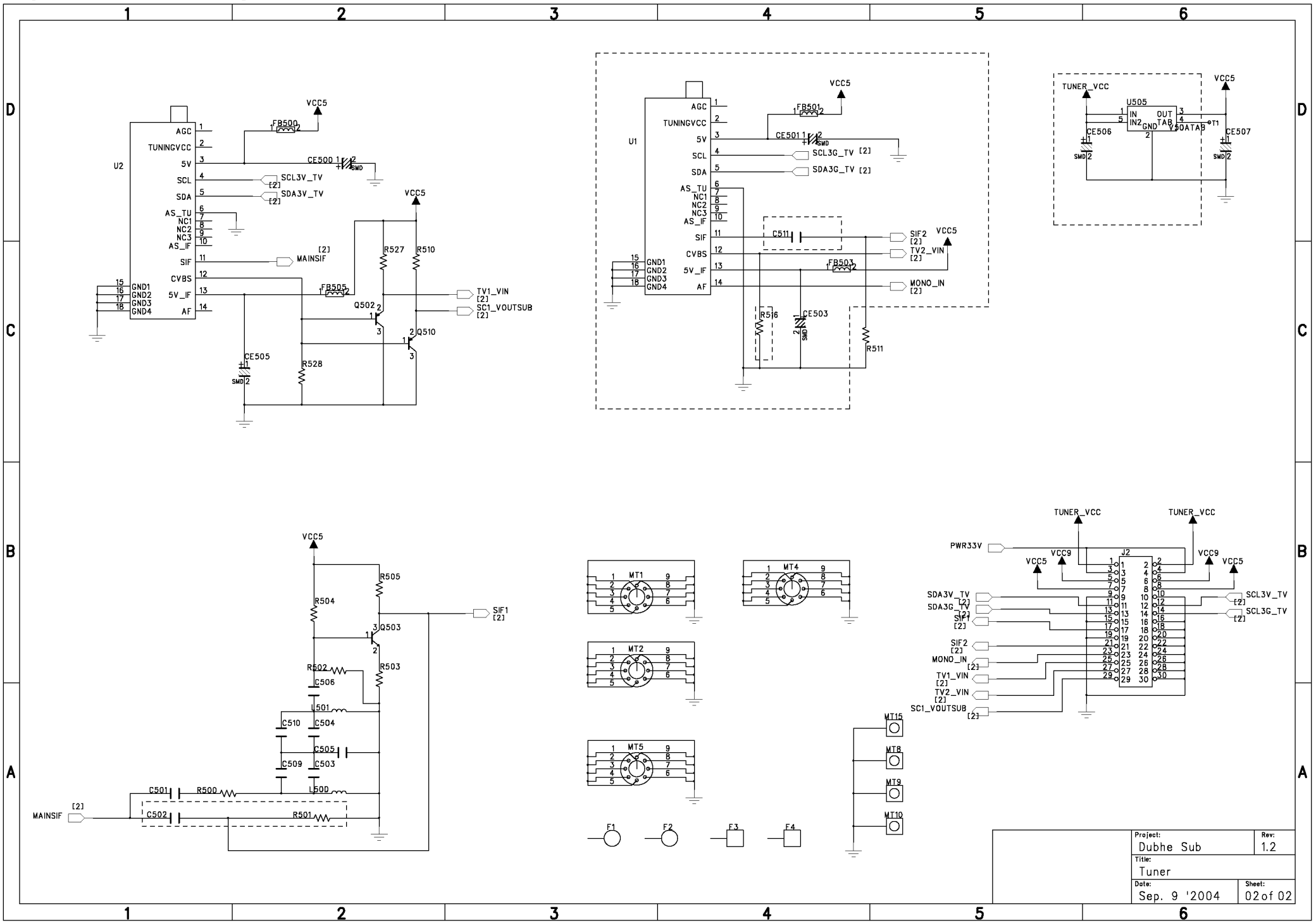






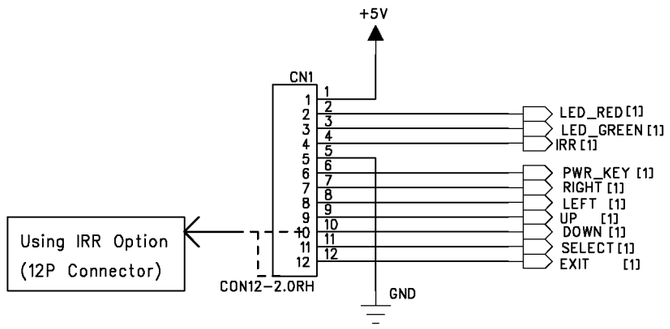
Project: Dubhe Sub		Rev: 1.2
Title: Tuner		
Date: Sep. 7 '2004	Sheet: 06 of 07	

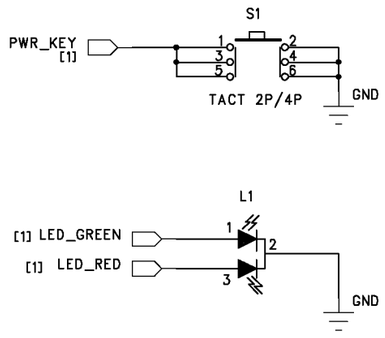

VCC5A
C608
U600
SC1_GIN [2]
SC1_RIN [2,3]
SC1_BIN [2]
SC1_BXIN [2]
S1A
S1B
S1C
S1D
S2A
S2B
S2C
S2D
VCC
DA
DB
DC
DD
IN
EN
GND
SC1_GRN [2]
SC1_RED [2]
SC1_BLU [2]
SC1_BOX [2]
SC_SEL [2]
SC2_GIN [2]
SC2_RIN [2,3]
SC2_BIN [2]
SC2_BXIN [2]
D610
D611
D612
D613
D614
D615
D616
D617
Project: Dubhe Sub
Rev: 1.2
Title: Scart Mux
Date: Sep. 7 '2004
Sheet: 07of 07

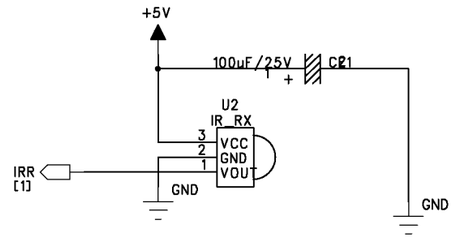


Project: Dubhe Sub	Rev: 1.2
Title: Tuner	
Date: Sep. 9 '2004	Sheet: 02of 02

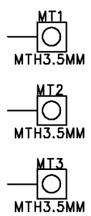
DUBHE OSD
6-Key OSD

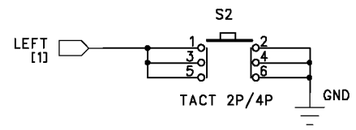


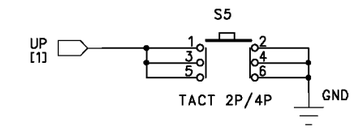


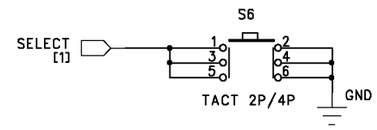


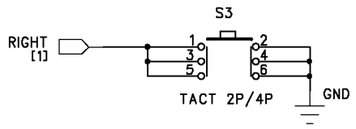
OSD I/F Connector

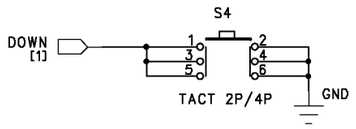


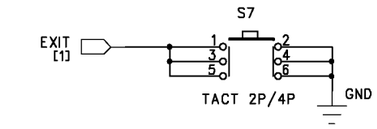






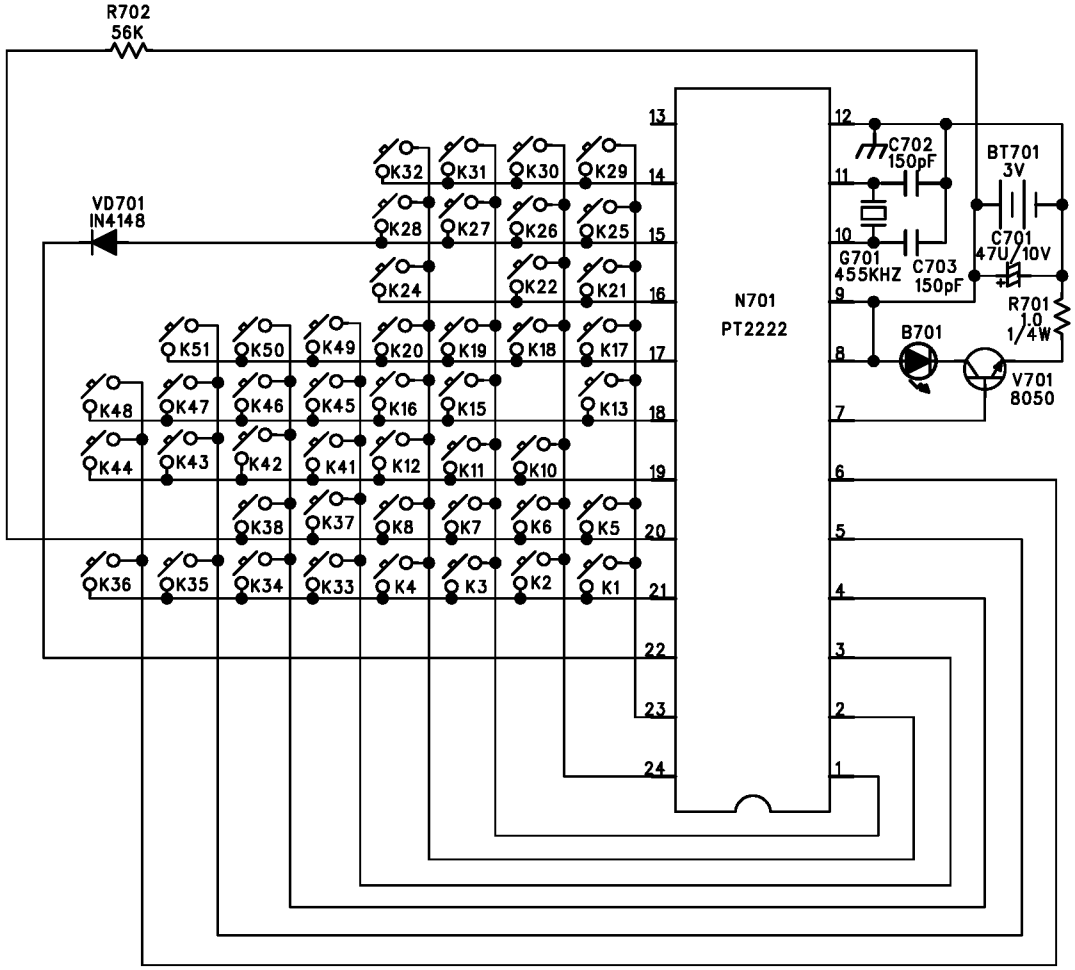






	Project: Project Name	Rev: 1.2
	Title: DUBHE OSD	
	Date: June. 15,2004	Sheet: xx of xx

REMOTE PCB



REMOTE CONTROL CODE ASSIGNMENT

KEY NO.	KEY NAME	DATA CODE	KEY NO.	KEY NAME	DATA CODE
K1	POWER	00	K33	dumb	40
K2	1	01	K34	dumb	41
K3	2	02	K35	dumb	42
K4	3	03	K36	dumb	43
K5	P.MODE	04	K37	MUTE	44
K6	4	05	K38	INFO	45
K7	5	06	K39	nil	46
K8	6	07	K40	nil	47
K9	nil	08	K41	100	48
K10	7	09	K42	PREV	49
K11	8	0A	K43	P.STILL	4A
K12	9	0B	K44	SOUND	4B
K13	MTS	0C	K45	SLEEP	4C
K14	nil	0D	K46	TIME	4D
K15	S.SELE	0E	K47	Picture	4E
K16	OK	0F	K48	CH Erase	4F
K17	CH.+	10	K49	CH Save	50
K18	VOL.+	11	K50	C/C	51
K19	VOL.-	12	K51	V-CHIP	52
K20	CH.-	13	K52	nil	53
K21	MENU	14	K53	nil	54
K22	Source	15	K54	nil	55
K23	nil	16	K55	nil	56
K24	P.SIZE	17	K56	nil	57
K25	0	18	K57	nil	58
K26	F.White	19	K58	nil	59
K27	PIP Source	1A	K59	nil	5A
K28	EXIT	1B	K60	nil	5B
K29	PIP	1C	K61	nil	5C
K30	SWAP	1D	K62	nil	5D
K31	PIP CH-	1E	K63	nil	5E
K32	PIP CH+	1F	K64	nil	5F

CUSTOM CODE: 20DD

FOR NTSC

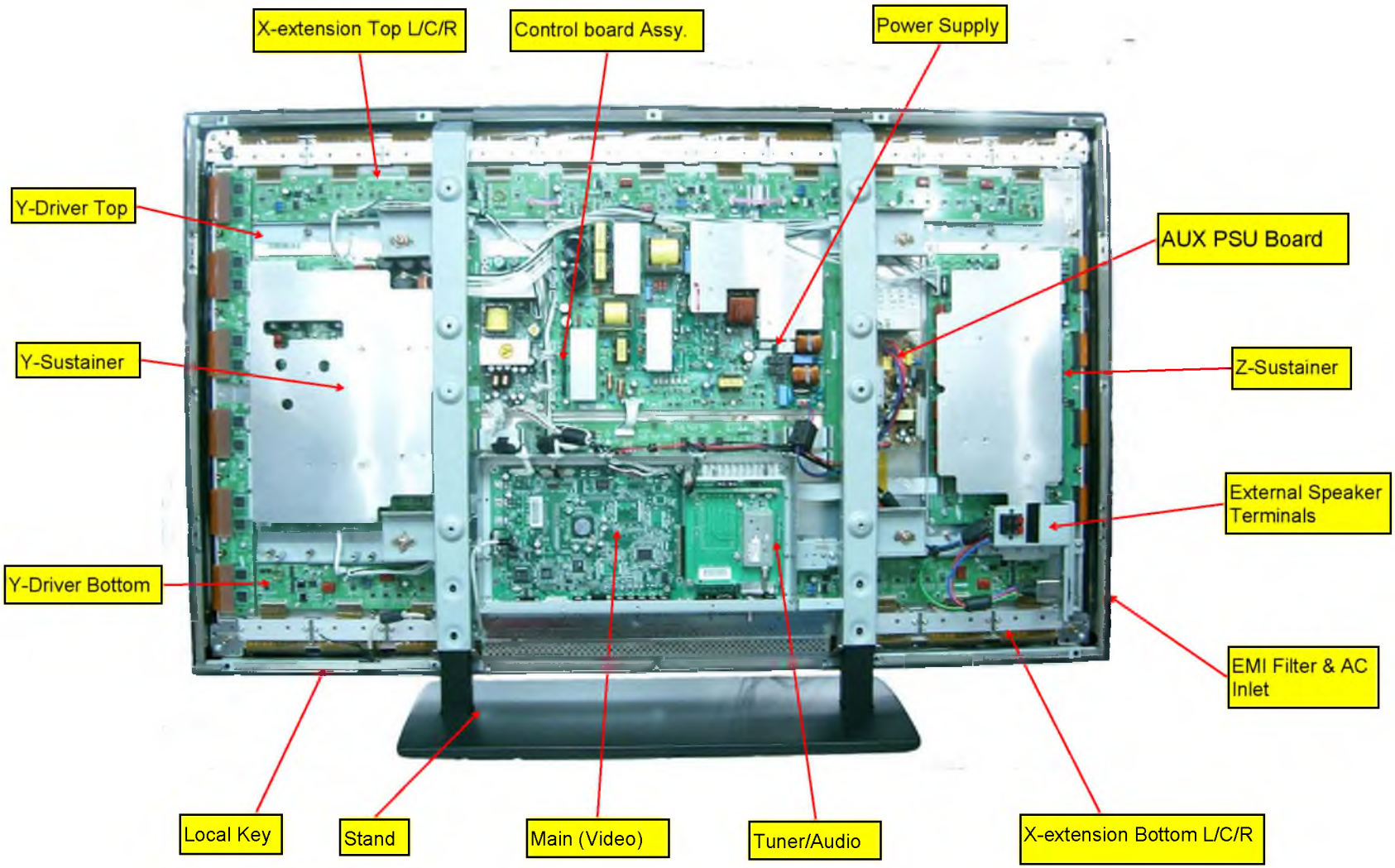
Basic Operations & Circuit Description

MODULE

There are 1 pc. panel and 12 pc.s PCB including 2 pc.s Y/Z Sustainer board, 2 pc.s Y Drive board, 6 pc.s X Extension boards, 1 pc. Control (Signal Input) and 1 pc. Power board in the Module.

SET

There are 6 pc.s PCBs including 1 pc. AUX. PSU Board, 1 pc. Keypad board, 1 pc. Remote Control Receiver board, 1 pc. L/R Speakers and 1 pc. Main (Video) board in the SET.


X-extension Top L/C/R
Control board Assy.
Power Supply
Y-Driver Top
AUX PSU Board
Y-Sustainer
Z-Sustainer
External Speaker Terminals
Y-Driver Bottom
EMI Filter & AC Inlet
Local Key
Stand
Main (Video)
Tuner/Audio
X-extension Bottom L/C/R

PCB function

1. Power:
   (1). Input voltage: AC 110V~240V, 47Hz~63Hz.
   Input range: AC 90V(Min)~265V(Max) auto regulation.
   (2). To provide power for PCBs.
2. Main (Video InterFace) board: To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI signals and D-SUB signals to digital ones and to transmit to Control board.
3. Control board: Dealing with the digital signal for output to panel.
4. Y-Sustainer / Z-Sustainer board:
   (1). Receiving the signals from Control and high voltage supply.
   (2). Output scanning waveform for Module.
5. Y-Drive board: Receive signal from Y sustainer, output horizontal scanning waveform to the panel.
6. X extension board (6pcs): Output addressing signals.
7. Tuner/Audio Board：Process and Amplifying the audio signal to speakers and convert TV RF signal to video/audio signal and send to Main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN (video) : a. Lacking color, Bad color scale.
   b. No voice.
   c. No picture but with signals output, OSD and back light.
   d. Abnormal noise on screen.
3. POWER : No picture, no power output.
4. Z - Sustainer : a. No picture.
   b. Color not enough.
   c. Flash on screen.
5. Y - Sustainer : Darker picture with signals.

6. X - Extension : Abormal vertical noise on screen.
7. Audio Board or AUX PSU: a. No voice. (Make sure Mute/OFF) .
   b. Noise.

Basic operation of Plasma Display

1. After turning on power switch, power board sends 5Vst-by Volt to Micro Processor

2. The micro Processor memorize the last state of Power, When the last state of power is on or receive power on signal from local Key or Remote control, Micro Processor will send on control signal to power. Then Power sends (5Vsc, 9Vsc, 24V and RLYON, Vs ON) to PCBs working. This time VIF will send signals to display Image, OSD on the panel and start to search available signal sources.
   If the audio signals input, them will be amplified by Audio AMP and transmitted to Speakers.

3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.

Main IC Specifications

- PW181 Image Processor, Scaler
- PW1231 Digital Video Signal Processor
- uPD64083 Three –Dimensional Y/C Separation LSI With On-Chip Memory
- AD9883A 110MSPS/140MSPS Analog Interface
- VPC 323XD Comb-filter Video Processor
- Si161B Panel Link Receiver
- Z86229 NTSC Line 21 CCD decorder
- MSP34x0G Multistandard Sound Processor

PW181

Product Specification

General Description

The PW181 ImageProcessor is a highly integrated "system-on-a-chip" that interfaces computer graphics and video inputs in virtually any format to a fixed-frequency flat panel display.

Computer and video images from NTSC/PAL to WUXGA at virtually any refresh rate can be resized to fit on a fixed-frequency target display device with any resolution up to WUXGA. Video data from 4:3 aspect ratio NTSC or PAL and 16:9 aspect ratio HDTV or SDTV is supported. Multi-region, nonlinear scaling allows these inputs to be resized optimally for the native resolution of the display.

Advanced scaling techniques are supported, such as format conversion using multiple programmable regions. Three independent image scalers coupled with frame locking circuitry and dual programmable color lookup tables create sharp images in multiple windows, without user intervention.

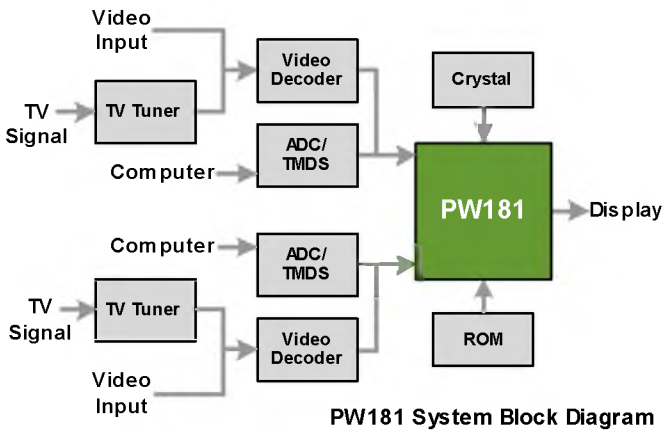
Embedded SDRAM frame buffers and memory controllers perform frame rate conversion and enhanced video processing completely on-chip. A separate memory is dedicated to storage of on-screen display images and CPU general purpose use.

Advanced video processing techniques are supported using the internal frame buffer, including motion adaptive, temporal deinterlacing with film mode detection. When used in combination with the new third-generation scaler, this advanced video processing technology delivers the highest quality video for advanced displays.

Both input ports support integrated DVI 1.0 content protection using standard DVI receivers.

A new advanced OSD Generator with more colors and larger sizes supports more demanding OSD applications, such as on-screen programming guides. When coupled with the new, faster, integrated microprocessor, this OSD Generator supports advanced OSD animation techniques.

Programmable features include the user interface, custom start-up screen, all automatic imaging features, and special screen effects.



PW181 System Block Diagram

Features

- Third-generation, two-dimensional filtering techniques
- Third-generation, advanced scaling techniques
- Second-generation Automatic Image Optimization
- Frame rate conversion
- Video processing
- On-Screen Display (OSD)
- On-chip microprocessor
- JTAG debugger and boundary scan
- Picture-in-picture (PIP)
- Multi-region, non-linear scaling
- Hardware 2-wire serial bus support

Applications

- Multimedia Displays
- Plasma Displays
- Digital Television

Device	Application	Package
PW181-10V	Up to XGA Displays	352 PBGA
PW181-20V	Up to UXGA Displays	

pixelworks

8100 SW Nyberg Road
Tualatin, OR 97062 USA
Telephone: 503.454.1750
FAX: 503.612.0848
www.pixelworks.com

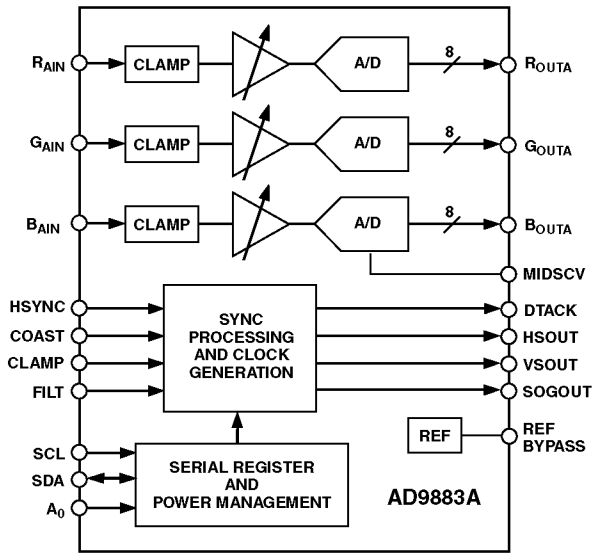
110 MSPS/140 MSPS Analog Interface for Flat Panel Displays

AD9883A

FEATURES
140 MSPS Maximum Conversion Rate
300 MHz Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
500 ps p-p PLL Clock Jitter at 110 MSPS
3.3 V Power Supply
Full Sync Processing
Sync Detect for "Hot Plugging"
Midscale Clamping
Power-Down Mode
Low Power: 500 mW Typical
4:2:2 Output Format Mode

APPLICATIONS
RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters
Microdisplays
Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9883A is a complete 8-bit, 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

REV. A

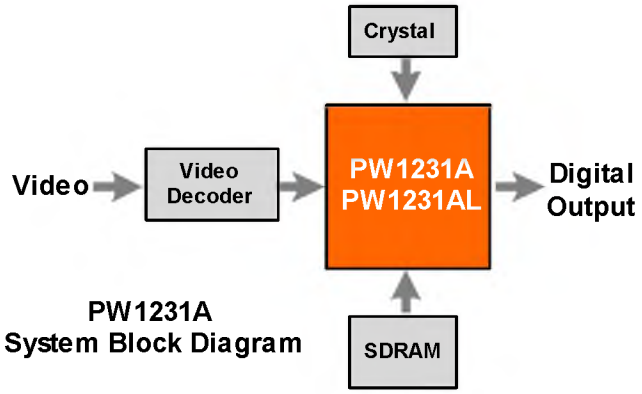
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel:
Fax:

PW1231A
Product Specification

General

The PW1231A is a high-quality, digital video signal processor that incorporates Pixelworks' patented deinterlacing, scaling, and video enhancement algorithms. The PW1231A accepts industry-standard video formats and resolutions, and converts the input into many desired output formats.The highly efficient video algorithms result in excellent quality video.

The PW1231A combines many functions into a single device, including a memory controller, auto-configuration, and others. This high level of integration enables simple, flexible, cost-effective solutions that require fewer components.



PW1231A
System Block Diagram

Features

- Built-In Memory Controller
- Motion-Adaptive Deinterlace Processor
- Intelligent Edge Deinterlacing
- Digital Color/Luminance Transient Improvement (DCTI/DLTI)
- Interlaced Video Input Options, including NTSC and PAL
- Independent horizontal and vertical scaling
- Copy Protection
- Two-Wire Serial Interface

Applications:
For use with Digital Displays

- Flat-Panel (LCD, DLP) TVs
- Rear Projection TVs
- Plasma Displays
- LCD Multimedia Monitors
- Multimedia Projectors

Device	Application	Package
PW1231A PW1231AL	Up to XGA	160-pin PQF

NOTE: "L" denotes lead (Pb) free

pixelworks

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www.pixelworks.com

P/N 001-0097-00 Rev B
July 2003

PRELIMINARY—CONFIDENTIAL

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD64083

THREE-DIMENSIONAL Y/C SEPARATION LSI WITH ON-CHIP MEMORY

DESCRIPTION

The μPD64083 realizes a high precision Y/C separation and a noise reduction by the three-dimension signal processing for NTSC signal.

This product has the On-chip 4-Mbit memory for flame delay, 2ch of high precision internal 10-bit A/D converter, and adapting 10-bit signal processing (only for luminance signal) and high picture quality. The μPD64083 is completely single-chip system of 3D Y/C separation.

This LSI includes the Wide Clear Vision ID signal (Japanese local format) decoder and ID-1 signal decoder.

FEATURES

- On-chip 4-Mbit frame delay memory.
- 4 Operation mode (Compatible to the μPD64082)
  - Motion adaptive 3D Y/C separation (for Composite video input)
  - Frame recursive Y/C NR (for Y/C separated video input)
  - Frame comb type YNR + 1H delayed C signal (for Y/C separated video input)
  - 2D Y/C separation + Frame recursive Y/C NR (for Composite video input)
- Embedded A/D converter (2ch), D/A converter (2ch), clock generator.
- Embedded Y coring, Vertical enhancer, Peaking filter, and Noise detector.
- Embedded WCV-ID decoder and ID-1 decoder.
- I^2C bus control.
- Dual power supply of 2.5 V and 3.3 V.
  - For digital : DV_{DD} = 2.5 V
  - For analog : AV_{DD} = 2.5 V
  - For DRAM : DV_{DDRAM} = 2.5 V
  - For I/O : DV_{DDIO} = 3.3 V

ORDERING INFORMATION

Part number	Package
μPD64083GF-3BA	100-pin plastic QFP (14 × 20)

Document No. S15849EJ1V0DS00 (1st edition)
Date Published January 2002 NS CP (K)
Printed in Japan

Comb Filter Video Processor

1. Introduction

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are

- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YC_rC_b component inputs, one Fast Blank (FB) input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panoramavision'
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface
- peaking, contrast, brightness, color saturation and tint for RGB/YC_rC_b and CVBS/S-VHS
- high-quality soft mixer controlled by Fast Blank
- PIP processing for four picture sizes ($\frac{1}{4}$, $\frac{1}{9}$, $\frac{1}{16}$, or $\frac{1}{36}$ of normal size) with 8-bit resolution
- 15 predefined PIP display configurations and expert mode (fully programmable)
- control interface for external field memory
- I^2C-bus interface
- one 20.25-MHz crystal, few external components
- 80-pin PQFP package

1.1. System Architecture

Fig.1–1 shows the block diagram of the video processor

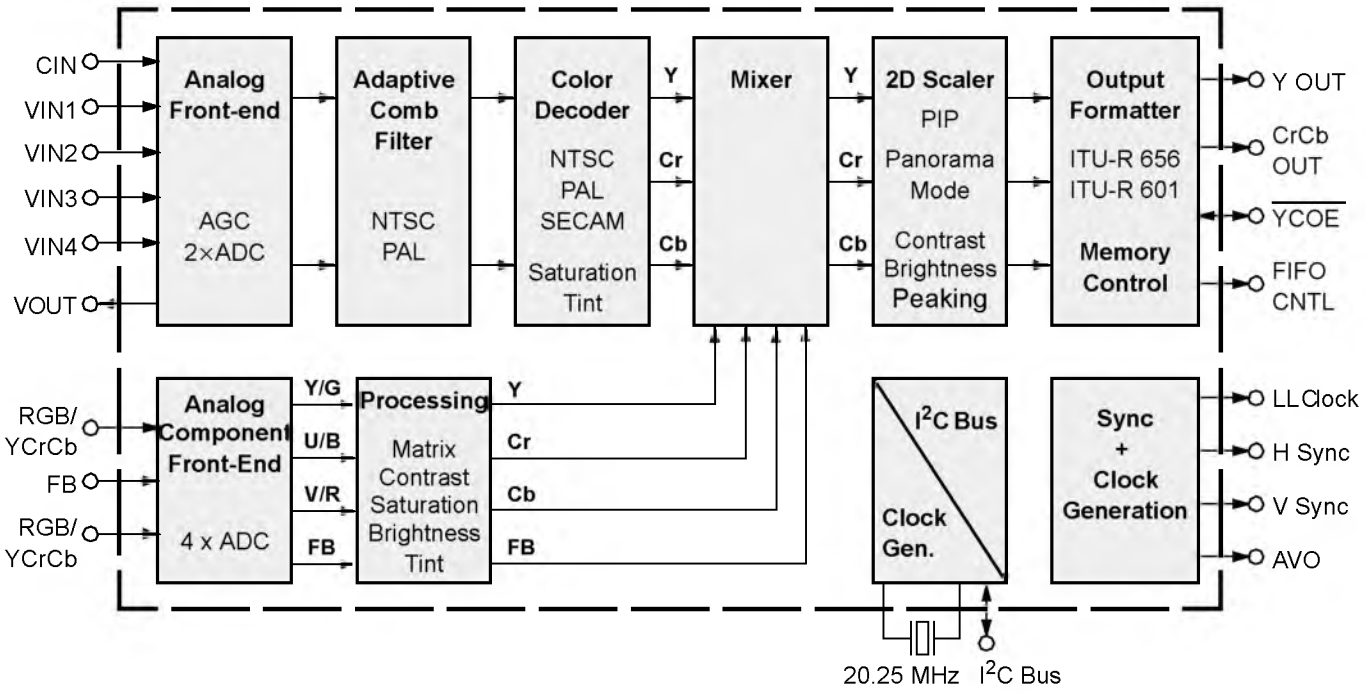


Fig. 1–1: Block diagram of the VPC 323xD

General Description

The SiI 161B receiver uses PanelLink Digital technology to support high-resolution displays up to UXGA (25-165MHz). This receiver supports up to true color panels (24 bits per pixel, 16M colors) with both one and two pixels per clock.

All PanelLink products are designed on a scaleable CMOS architecture, ensuring support for future performance enhancements while maintaining the same logical interface. System designers can be assured that the interface will be stable through a number of technology and performance generations.

PanelLink Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Low Power Operation: 280mA max. current consumption at 3.3V core operation
- Time staggered data output for reduced ground bounce and lower EMI
- Sync Detect feature for Plug & Display
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- ESD tolerant to 5kV (HBM on all pins)
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™, FPDI-2™ and DFP)
- HSYNC de-jitter circuitry enables stable operation even when HSYNC contains jitter
- Low power standby mode
- Automatic entry into standby mode with clock detect circuitry
- Standard and Pb-free packages (see page 25).

ZiLOG

Totally Logical

Z86229

NTSC LINE 21 CCD DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	On-Screen Display & Closed Captioning	Automatic Data Extraction: Program Rating	Automatic Data Extraction: Time of Day
Z86229	12	18-Pin DIP, SOIC	0°C to +70°C	Yes	Yes	Yes

- Complete Stand-Alone Line 21 Decoder for Closed-Captioned and Extended Data Services (XDS)
- Preprogrammed to Provide Full Compliance with EIA–608 Specifications for Extended Data Services
- Automatic Extraction and Serial Output of Special XDS Packets (Time of Day, Local Time Zone, and Program Blocking)
- Programmable XDS Filter for a Specific XDS Packet
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows
- Minimal Communications and Control Overhead Provide Simple Implementation of Violence Blocking, Closed Captioning, and Auto Clock Set Features
- Programmable, On-Screen Display (OSD) for Creating Full Screen OSD or Captions inside a Picture-in-Picture (PiP) Window
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment
- I^2C Serial Data and Control Communication
- Supports 2 Selectable I^2C Addresses

GENERAL DESCRIPTION

Capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data, the Z86229 Line 21 Decoder offers a feature-rich solution for any television or set-top application. The robust nature of the Z86229 helps the device conform to the transmission format defined in the Television Decoder Circuits Act of 1990, and in accordance with the Electronics Industry Association specification 608 (EIA–608).

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 consists of four data channels: two Captions and two Texts. Field 2 consists of five additional data channels: two Captions, two Texts, and Extended Data Services (XDS). The XDS data structure is defined in EIA–608. The Z86229 can recover and display data transmitted on any of these nine data channels.

The Z86229 can recover and output to a host processor via the I^2C serial bus. The recovered XDS data packet is further defined in the EIA–608 specification. The on-chip XDS filters in the Z86229 are fully programmable, enabling recovery of only those XDS data packets selected by the user. This functionality allows the device to extract the required XDS information with proper XDS filter setup for compatibility in a variety of TVs, VCRs, and Set-Top boxes.

In addition, the Z86229 is ideally suited to monitor Line 21 video displayed in a PiP window for violence blocking, CCD, and other XDS data services. A block diagram of the Z86229 is illustrated in Figure 1.

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x0G version B8 and following versions.

1. Introduction

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I^2C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).

The MSP 34x0G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x0G is available in the following packages: PLCC68 (not intended for new design), PSDIP64, PSDIP52, PQFP80, and PLQFP64.

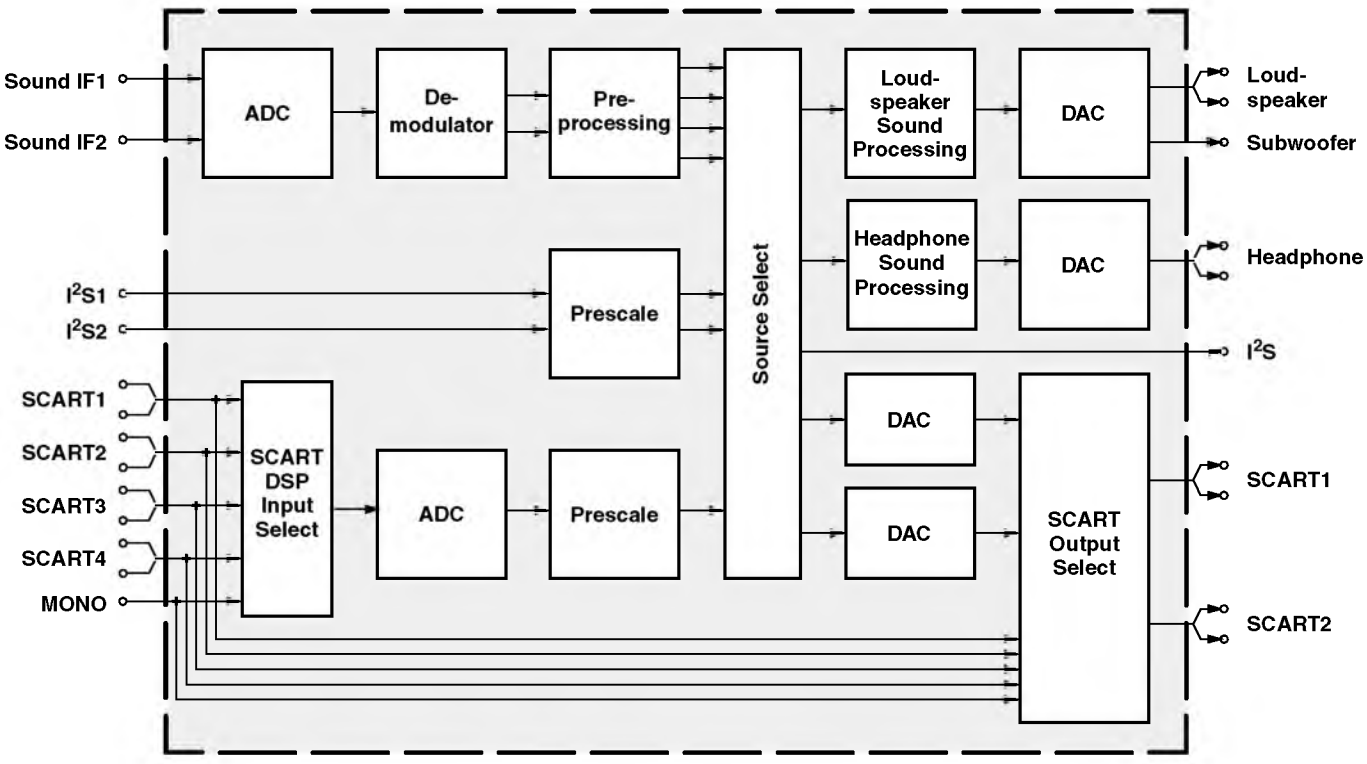


Fig. 1–1: Simplified functional block diagram of the MSP 34x0G

MODEL : 50'' HD D3.1 PDP

1,269cm (50 Inch) Wide Plasma Display Module

Quality innovation Team

CONTENTS

Formation and Specification of Module

1. Overview

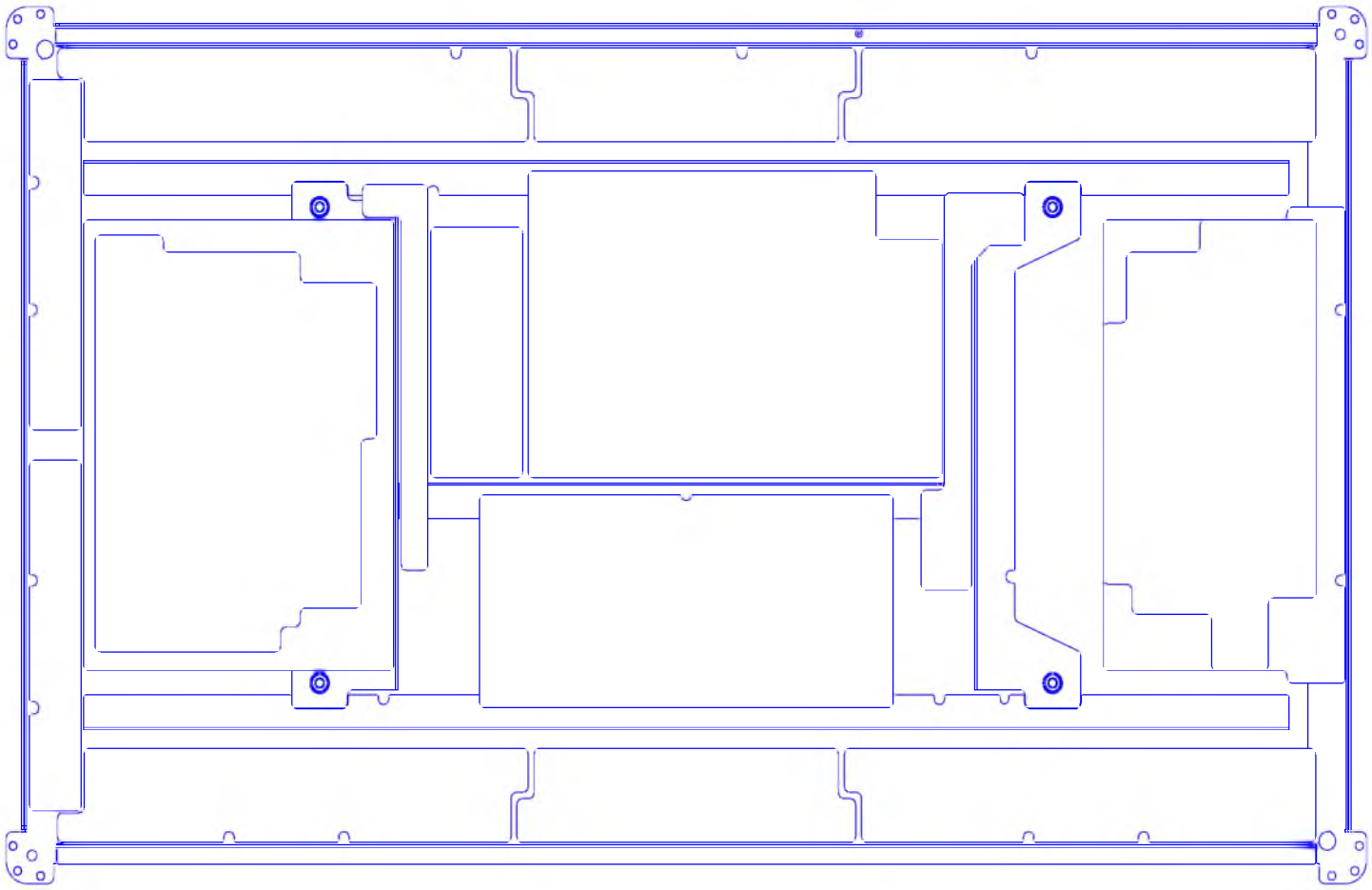
1-1 Model Name of Plasma Display

MODEL : 50HD" D3.1 PDP (S50HW-XD03)

1-2 External View

【 M3 = X Board + Y Board + Logic Board + PSU + SUB PSU 】

1-3 Points of Screw Mount



Blue Dot : SCREW 4X12

Red Dot : SCREW 3X10

1-4 Specifications

No	Item	Specification	
1	Pixel	Horizontal 1366 × Vertical 768 pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	Horizontal 4,098 × Vertical 768 cells	
3	Pixel Pitch	Horizontal 810㎛ × Vertical 810㎛	
4	Cell Pitch	R	Horizontal 270㎛ × Vertical 810㎛
		G	Horizontal 270㎛ × Vertical 810㎛
		B	Horizontal 270㎛ × Vertical 810㎛
5	Display size	Horizontal 1106.46㎜ × Vertical 622.08㎜	
6	Screen size	Diagonal 50" Color Plasma Display Module	
7	Screen aspect	16 : 9	
8	Display color	16.77 million colors	
9	Viewing angle	Over 160° (Angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1184(W) × 700 (H) × 60.1 (D) ㎜	
11	Weight	Module 1	About 18.0 kg
12	Packing weight	Module 1	140kg ± 5kg (including modules) / 5pcs/BOX
13	Packing size	L 760 * W 1465 * H 1106(mm) / 10pcs/BOX	
14	Broadcasting reception Vertical frequency and Video/Logic Interface		60Hz/ 50Hz, LVDS

2. Precaution

**** To prevent the risks of unit damage, electrical shock and radiation, take the following safety, service, and ESD precautions.**

2-1 Handling Precautions for Plasma Display

- PDP module use high voltage that is dangerous to human. Before operating PDP, always check the dust to prevent circuit short. Be careful touching the circuit device when power is on.
- PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- PDP module has a lot of electric devices. Service engineer must wear equipment(for example , earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. Operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is off. Operator must wait for discharging of remaining voltage during at least 1 minute.

2-2 Safety Precautions for Service (Handling, prevention of a electrical shock, measure against power outage, etc)

(Safety Precautions)

- Before replacing a board, discharge forcibly The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operatior
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.

- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuffs including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change : Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, It cause danger on safety. And, If you change the design or insert, Manufactor guarantee will be not effect. .
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark : Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned off, before next repair..
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

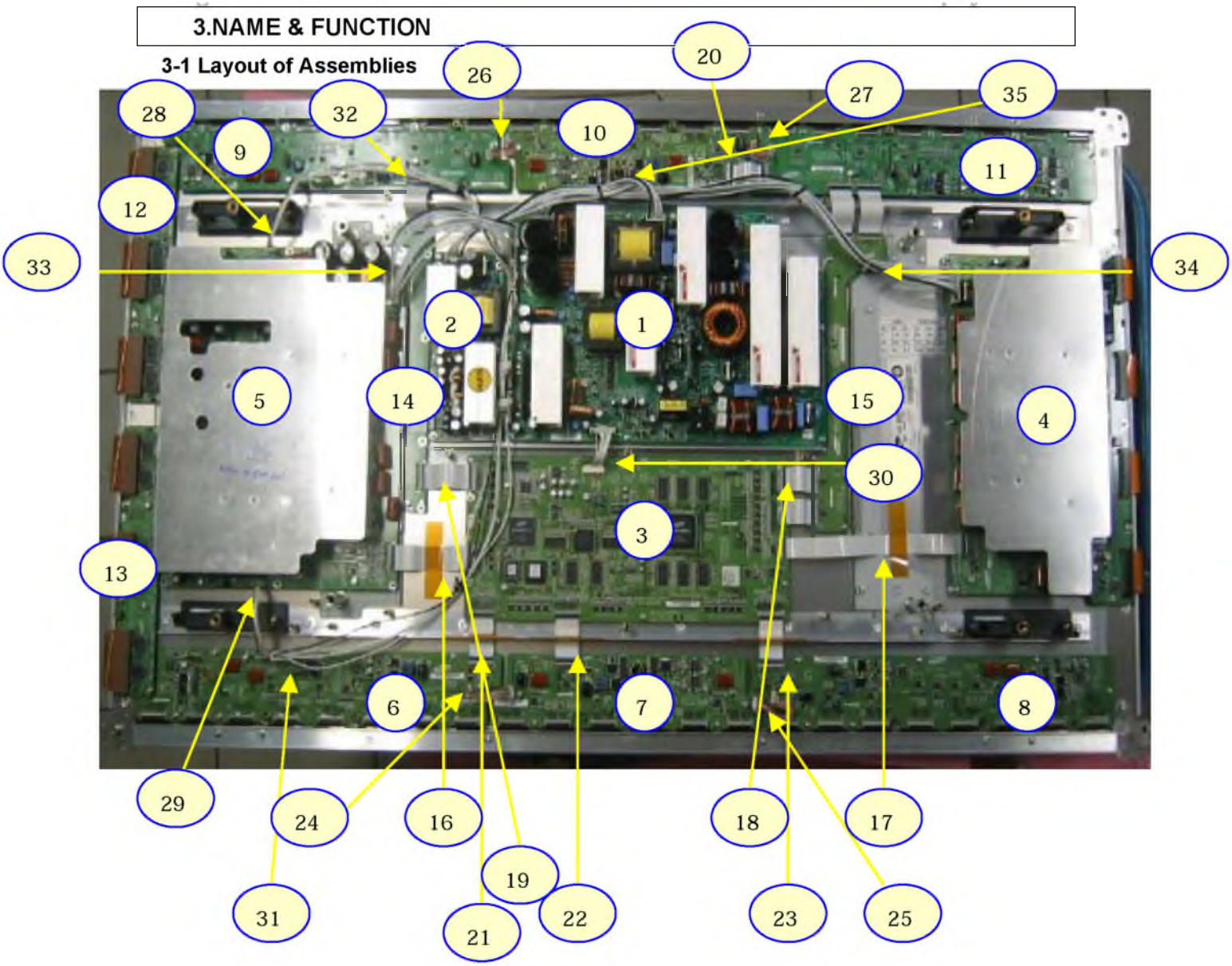
(Precaution when repairing ESD)

- There is ESD which is easily damaged by electrostatics.(for example Integrated circuit, FET) Electrostatic damage rate of product will be reduced by the following technics
- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring. (It must be operated after removing dust on it – It comes under precaution of electric shock.)

- After removing ESD assembly, put on it with aluminum stuff on the conductive surface to prevent charging.
- Do not use chemical stuff using Freon. It generates positive electric that can damage ESD.
- Must use a soldering device for ground-tip when soldering or de-soldering ESD.
- Must use anti-static solder removal device. Most removal device do not have antistatic which can charge a enough positive electric enough damaging ESD.
- Before removeing the protective material from the lead of a new ESD, bring the protective material into contact with the chassis or assembly that the ESD is to be installed on.
- When handing an unpacked ESD for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the ESD.
- Do not take a new ESD from the protective case until the ESD is ready to be installed. Most ESD have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminum)

3.NAME & FUNCTION

3-1 Layout of Assemblies



No.	Code No.	Location	Name
1	LJ44-00065A	Main PUS	ASSY PCB PSU
2	LJ44-00099A	SUB-PSU	ASSY PCB SUB-PSU
3	LJ92-00949C	LOGIC-MAIN Board	ASSY PCB LOGIC MAIN
4	LJ92-00852A	X-MAIN Driving Board	ASSY PCB X MAIN
5	LJ92-00853A	Y-MAIN Driving Board	ASSY PCBY MAIN
6	LJ92-00917A	LOGIC E BUFFER Board	ASSY PCB BUFFER
7	LJ92-00918A	LOGIC F BUFFER Board	ASSY PCB BUFFER
8	LJ92-00919A	LOGIC G BUFFER Board	ASSY PCB BUFFER
9	LJ92-00920A	LOGIC H BUFFER Board	ASSY PCB BUFFER
10	LJ92-00921A	LOGIC I BUFFER Board	ASSY PCB BUFFER
11	LJ92-00922A	LOGIC J BUFFER Board	ASSY PCB BUFFER
12	LJ92-00880A	Y-BUFFER (UPPER) Board	ASSY PCB BUFFER
13	LJ92-00881A	Y-BUFFER (DOWN) Board	ASSY PCB BUFFER
14	LJ92-00959A	SUB-R	ASSY PCB BUFFER
15	LJ92-00923A	SUB-L	ASSY PCB BUFFER
16	3809-001526	LOGIC + Y-MAIN	FFC CABLE-FLAT
17	3809-001516	LOGIC + X-MAIN	FFC CABLE-FLAT
18	3809-001414	SUB R + LOGIC	FFC CABLE-FLAT
19	3809-001414	SUB L + LOGIC	FFC CABLE-FLAT
20	3809-001414	LOGIC BUF(I) + LOGIC BUF(J) (UP)	FFC CABLE-FLAT
21	3809-001415	LOGIC + LOGIC BUF(E)(Down)	FFC CABLE-FLAT
22	3809-001415	LOGIC + LOGIC BUF(F)(Down)	FFC CABLE-FLAT
23	3809-001415	LOGIC + LOGIC BUF(G)(Down)	FFC CABLE-FLAT
24	LJ39-00121A	LOGIC BUF(E) + LOGIC BUF(F)	LEAD CONNECTOR
25	LJ39-00121A	LOGIC BUF(F) + LOGIC BUF(G)	LEAD CONNECTOR
26	LJ39-00121A	LOGIC BUF(H) + LOGIC BUF(I)	LEAD CONNECTOR
27	LJ39-00121A	LOGIC BUF(I) + LOGIC BUF(J)	LEAD CONNECTOR
28	LJ39-00122A	Y-MAIN + LOGIC BUF(H)	LEAD CONNECTOR
29	LJ39-00122A	Y-MAIN + LOGIC BUF(E)	LEAD CONNECTOR
30	LJ39-00113A	PSU + LOGIC MAIN	LEAD CONNECTOR
31	LJ39-00118A	PSU + LOGIC BUF(E)	LEAD CONNECTOR
32	LJ39-00177A	PSU + LOGIC BUF(H)	LEAD CONNECTOR
33	LJ39-00175A	PSU + Y-MAIN	LEAD CONNECTOR
34	LJ39-00173A	PSU + X-MAIN	LEAD CONNECTOR
35	LJ39-00178A	PSU + SUB PSU	LEAD CONNECTOR

1. L-Main	2.X-Main
	
3. Y-Main	**3. E-Buffer**
	
4, F-Buffer	**5. G-Buffer**
	
7. H-Buffer	**8. I-Buffer**
	

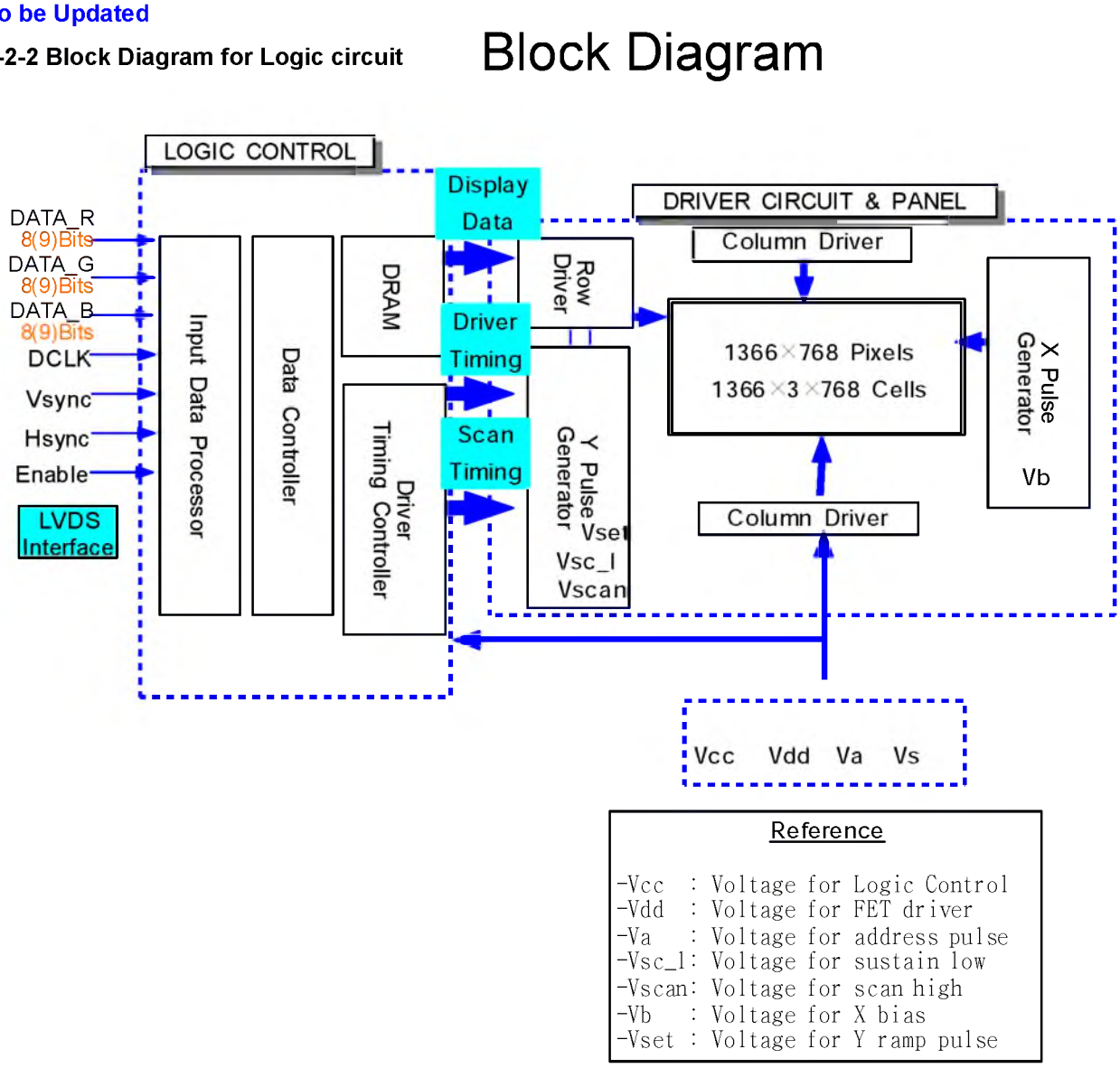
9. J-Buffer	10. Y-Buffer (lower)
	
11. Y-Buffer (Down)	**12. Sub-R**
	
13. Sub-L	
	

3-2 BLOCK DIAGRAM

3-2-1 BLOCK DIAGRAM FOR DRIVE CIRCUIT OPERATION

To be Updated

3-2-2 Block Diagram for Logic circuit



3-3 Main function of Each Assembly

■ X-main board : The X-main board generate a drive signal by switching the FET in synchronization with logic main board timing and supplies the X electrode of the panel with the drive signal through the connector.

1) Maintain voltage waveforms (including ERC)
2) Generate X rising ramp signal
3) Maintain Ve bias between Scan intervals

■ Y-main board : The Y-main board generate a drive signal by switching the FET in synchronization with the logic Main Board timing and sequentially supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1) Maintain voltage waveforms (including ERC)

2) Generate Y-rising Falling Ramp

3) Maintain V scan bias

■ Logic main board : The logic main board generates and outputs the address drive output signal and the X ,Y drive signal by processing the video signals. This Board buffers the address dirve output signal and feeds it to the address drive IC (COF module)

(video signal- X Y drive signal generation , frame memory circuit / address data rearrangement)

■.Logic buffer(E,F) : The logic buffer transmits data signal and control signal.

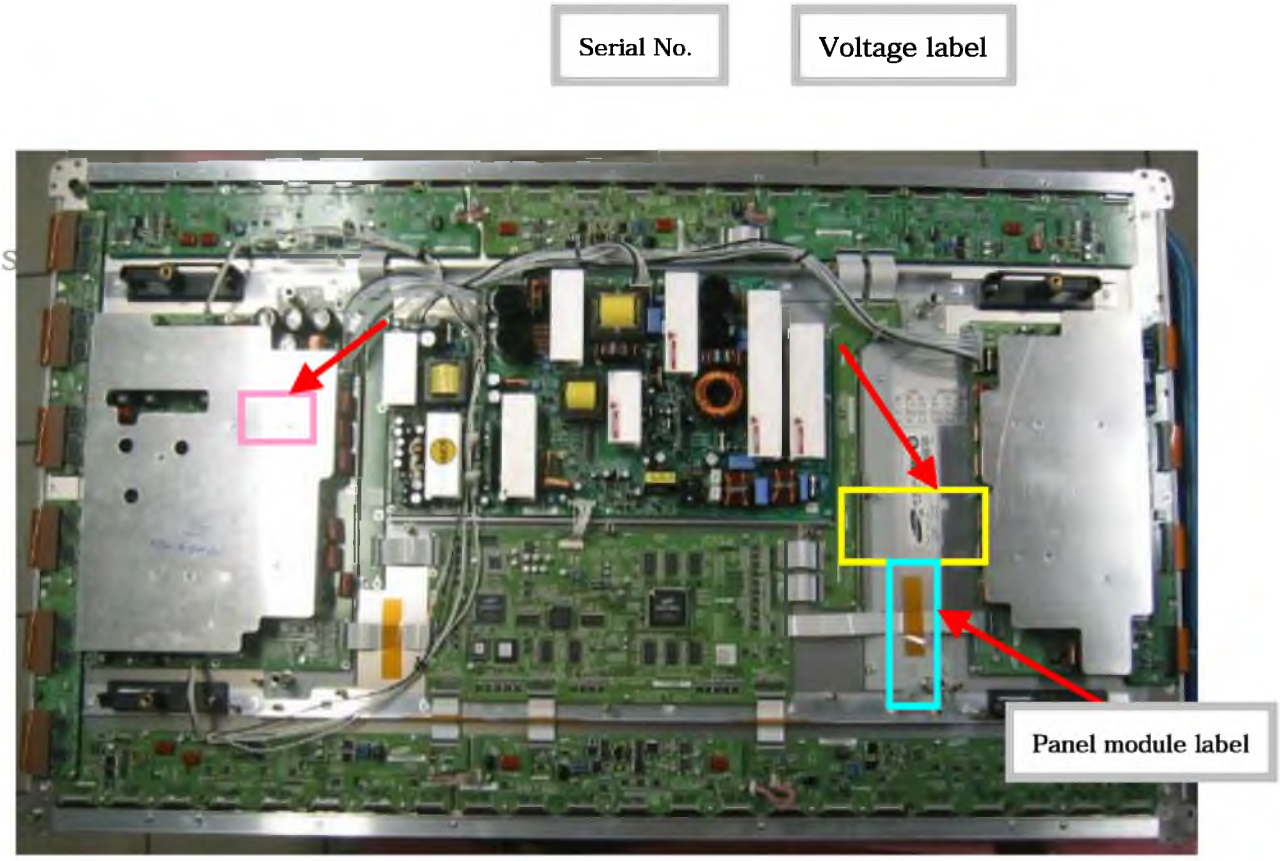
■.Y-buffer board (Upper, Lower) : The Y-buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises 8 scan driver IC's (ST microelectronics STV 7617 : 64 or 65 output pins) , but 4 ICs for the SD class

■.AC Noise Filter : The AC Noise filter has function for removing noise(low Frequency) and blocking surge. It effects Safety standards(EMC,EMI)

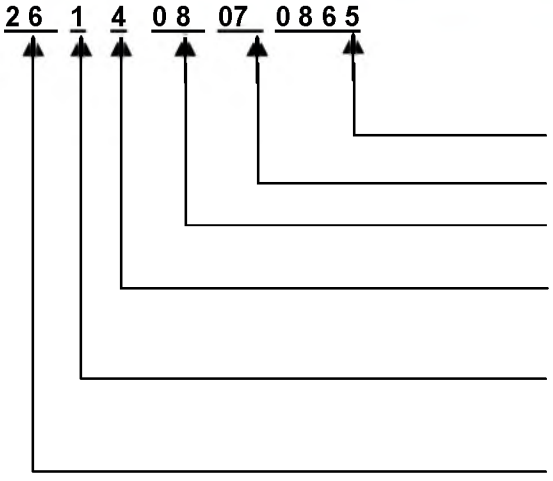
■.TCP(Tape Carrier Package) : The TCP applies Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise 4 data driver Ics(STV7610A :96 pins output pins) 7 TCPs are required for signal scan

.

3-4 PRODUCT/ SERIAL LABEL LOCATION



3-4-1 Serial No.



Serial No : 0001~9999
Date : 01~31
Month : 01~12
Year : 00(2000) ~99(2099)
Line No : 1 ~ 9 (0:Pilot Line)
Type : 02~48 **(ex.50HDv3:26)** (Step of even)

4. OPERATION CHECKING AFTER RECTIFICATION

4-1 Flow chart

* A/S Check Point *

1.Checking the voltage for each assembly

↓

2. Judging the Logic board working or not [Vsync, 3.3V, 5V]

↓

3. Adjusting the output signal through test points

↓

4. Checking the panel's crack

4-1-1 No voltage output

Check CN8001/2pin
Connect [220Vac]
LED 8004;Green

Ac Input

NG → Reconnect it

OK

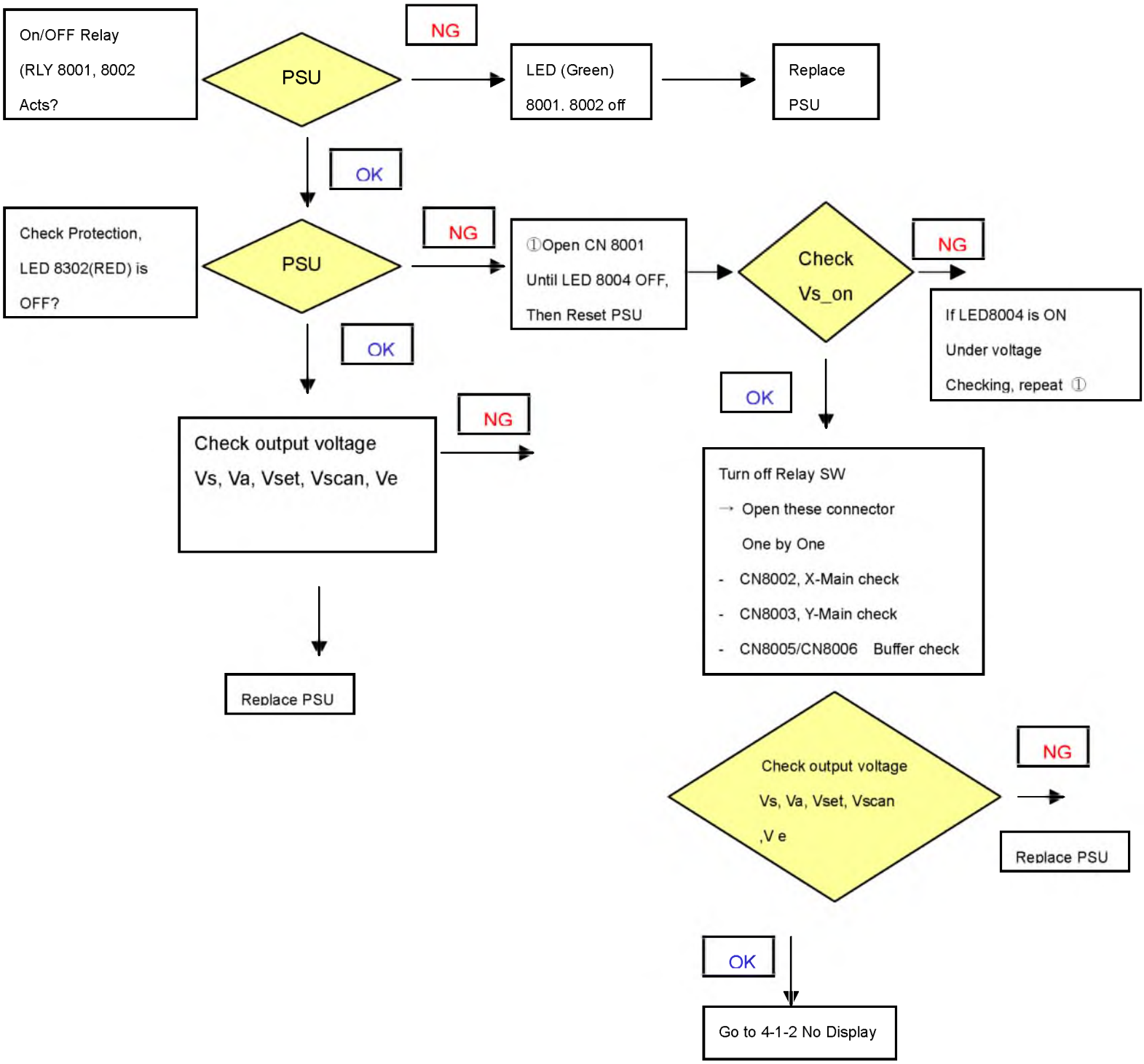
Check
LED 8001,8002
Green

①PSU

NG →

PSU Voltage check

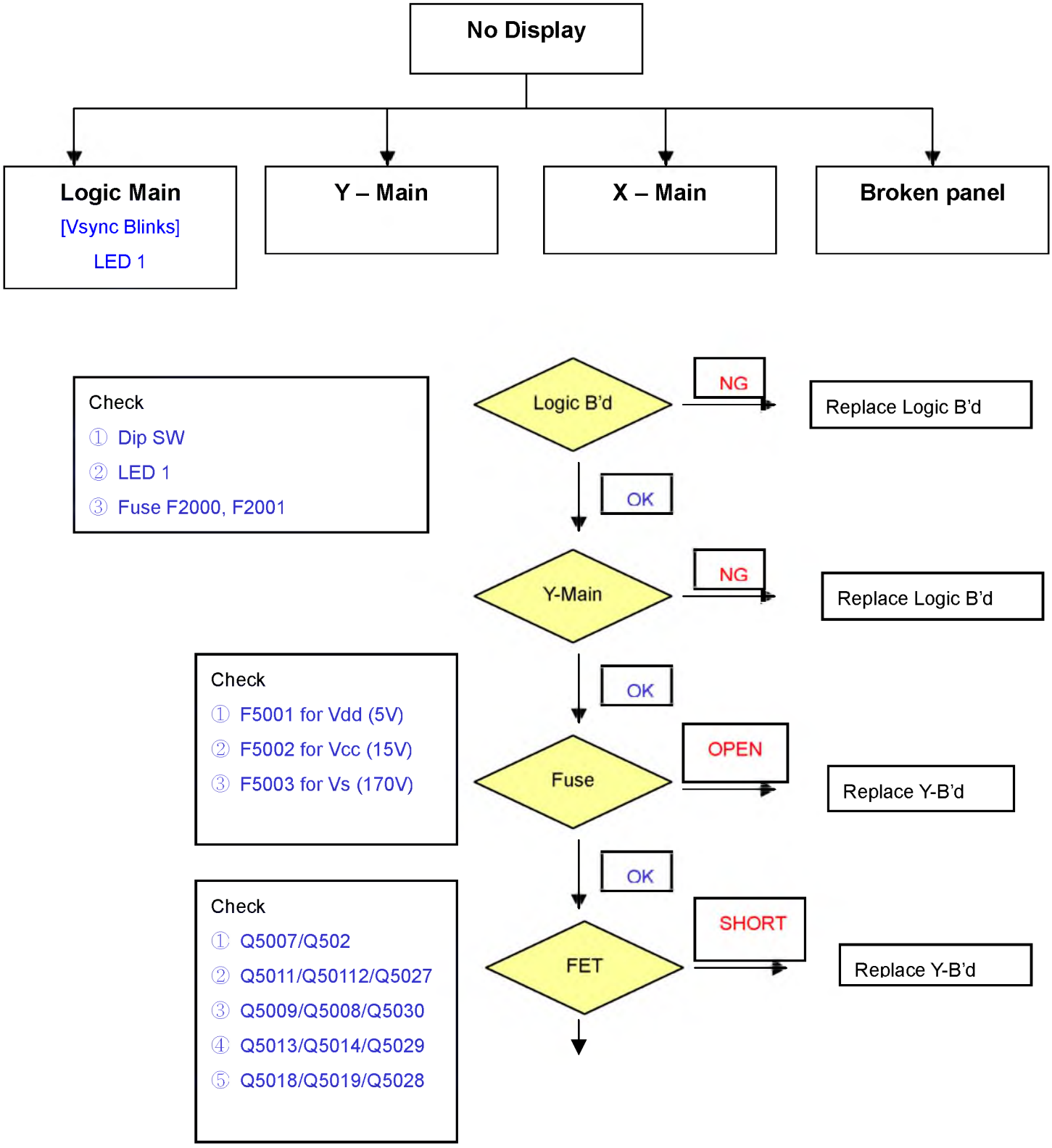
D5V; 5V Check
Vs ; 170V Check
Va ; 72V Check
Vset; 180V Check
Vscan; -90V Check
Vb; 155V Check
Vcc; 15V Check
Vcan_h; 25V Check
D3V3; 3.3V Check
9Vstandby;9V Check
Fuse 8001/8002/8003

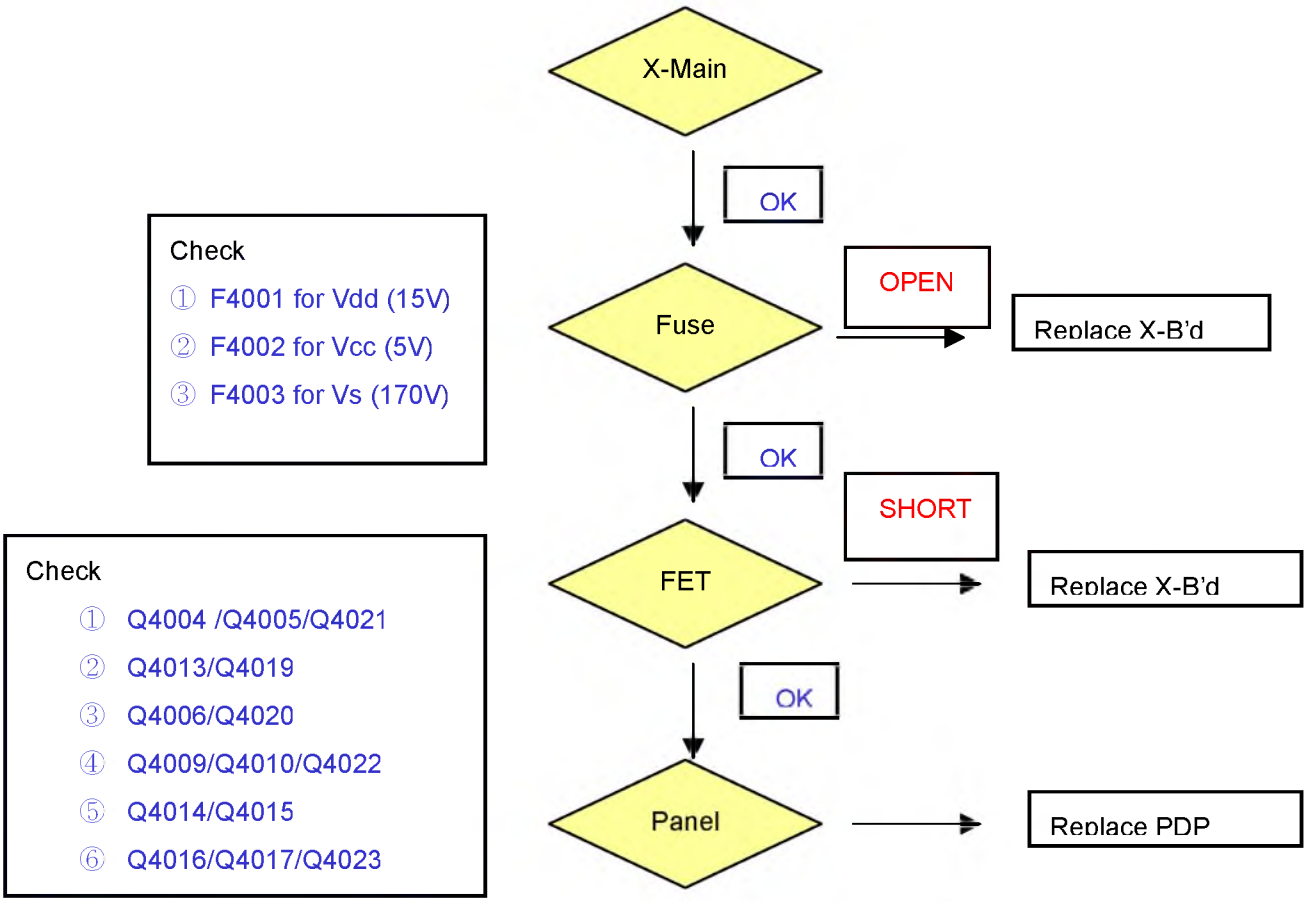

On/OFF Relay
(RLY 8001, 8002
Acts?
PSU
NG
LED (Green)
8001. 8002 off
Replace
PSU
OK
Check Protection,
LED 8302(RED) is
OFF?
PSU
NG
①Open CN 8001
Until LED 8004 OFF,
Then Reset PSU
Check
Vs_on
NG
If LED8004 is ON
Under voltage
Checking, repeat ①
OK
OK
Check output voltage
Vs, Va, Vset, Vscan, Ve
NG
Turn off Relay SW
→ Open these connector
One by One
- CN8002, X-Main check
- CN8003, Y-Main check
- CN8005/CN8006 Buffer check
Replace PSU
Check output voltage
Vs, Va, Vset, Vscan
,V e
NG
Replace PSU
OK
Go to 4-1-2 No Display

4-1-2 NO display (operating Voltage but an image doesn't exist on Screen)

⇒ No Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.

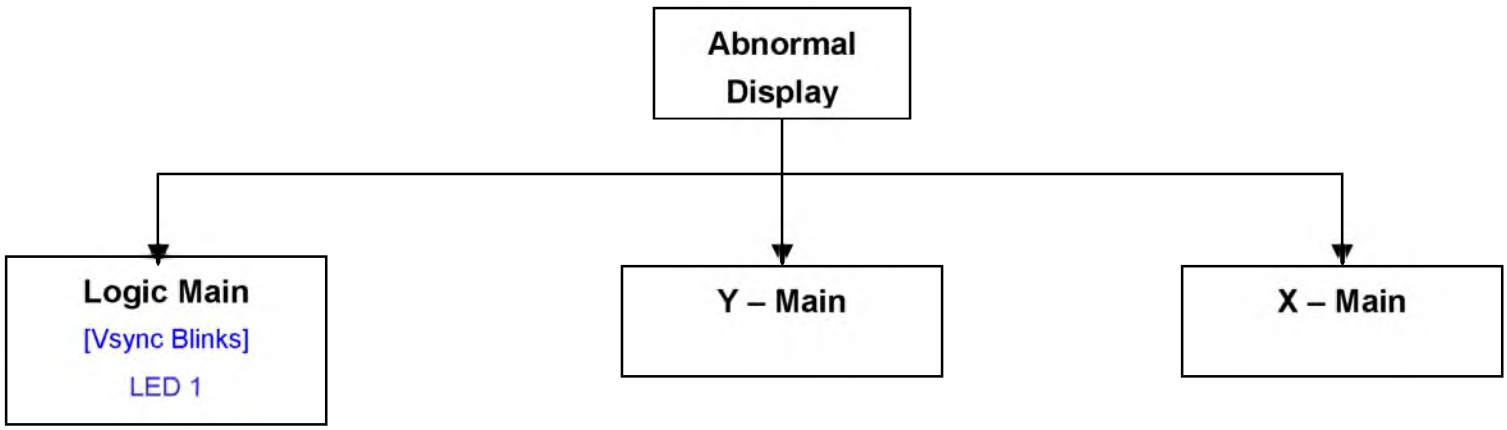


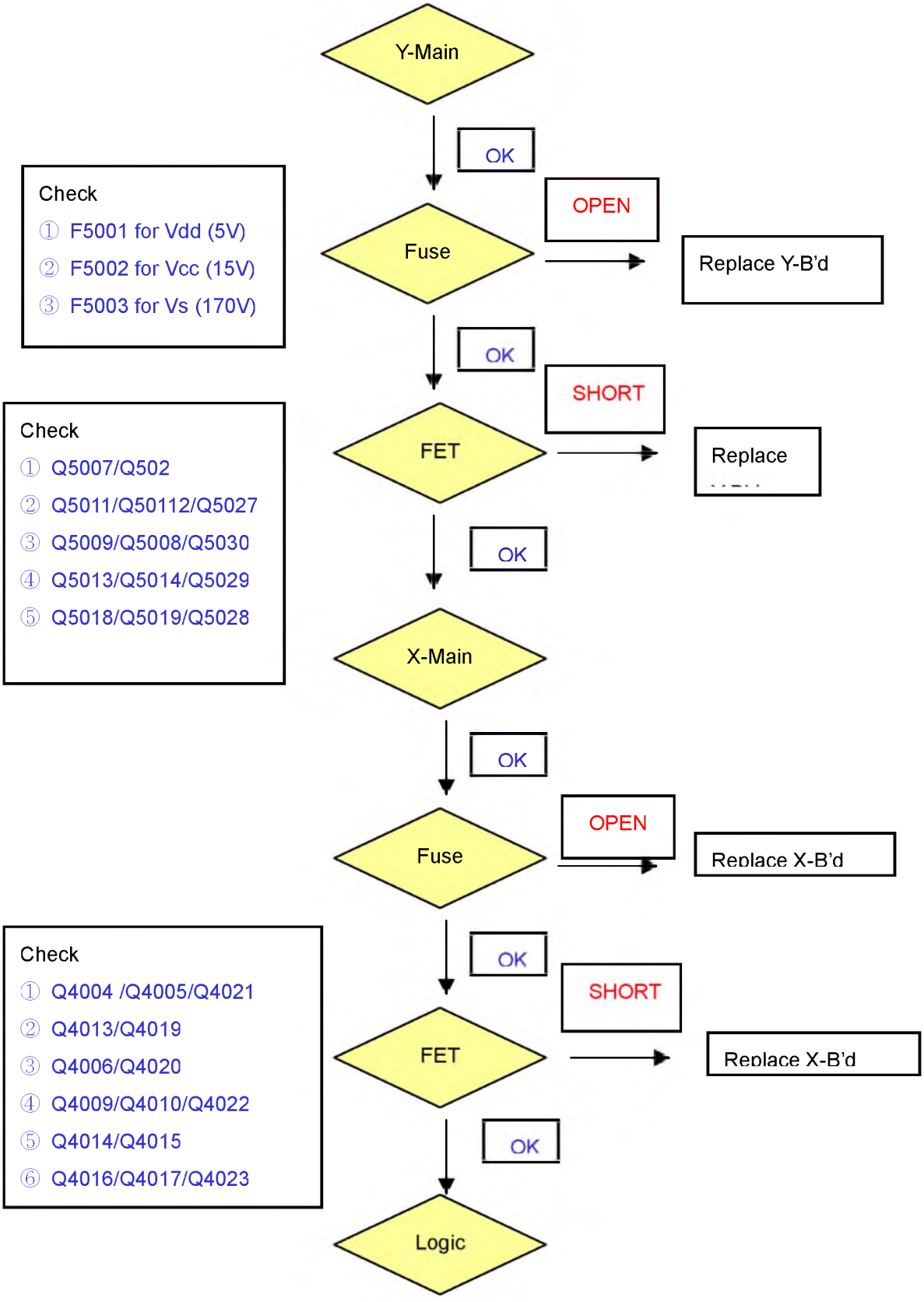


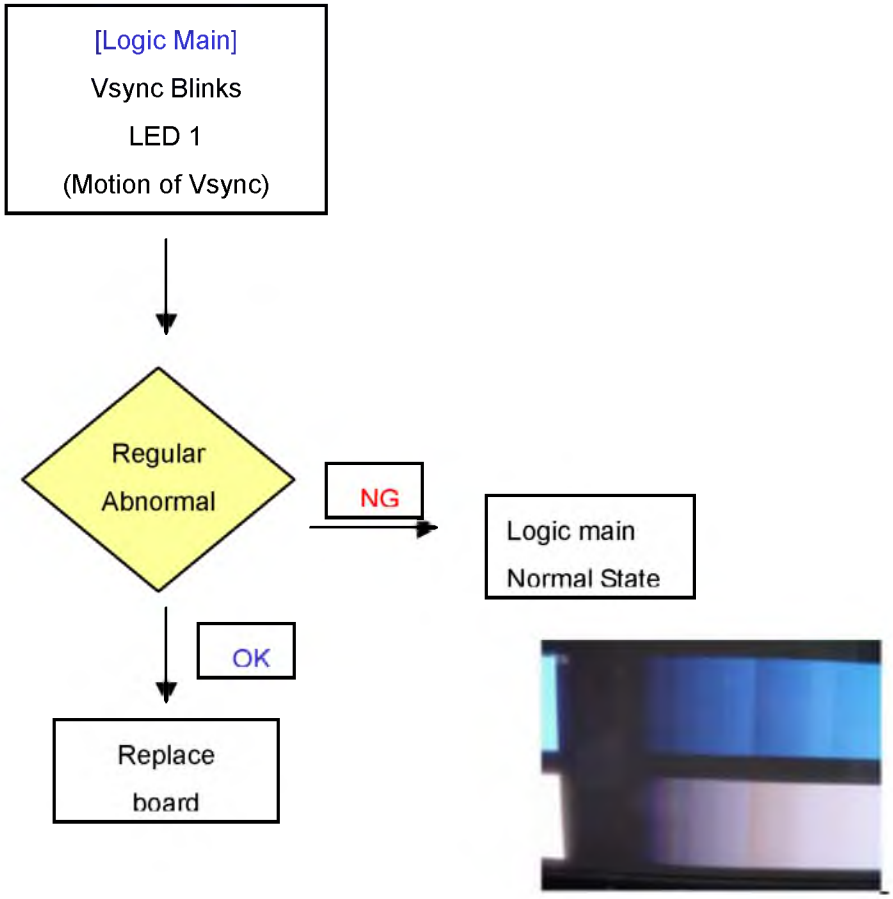
4-1-3 Abnormal Display (Abnormal Image is on Screen. (except abnormality in Sustain or Address)

⇒ Abnormal Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

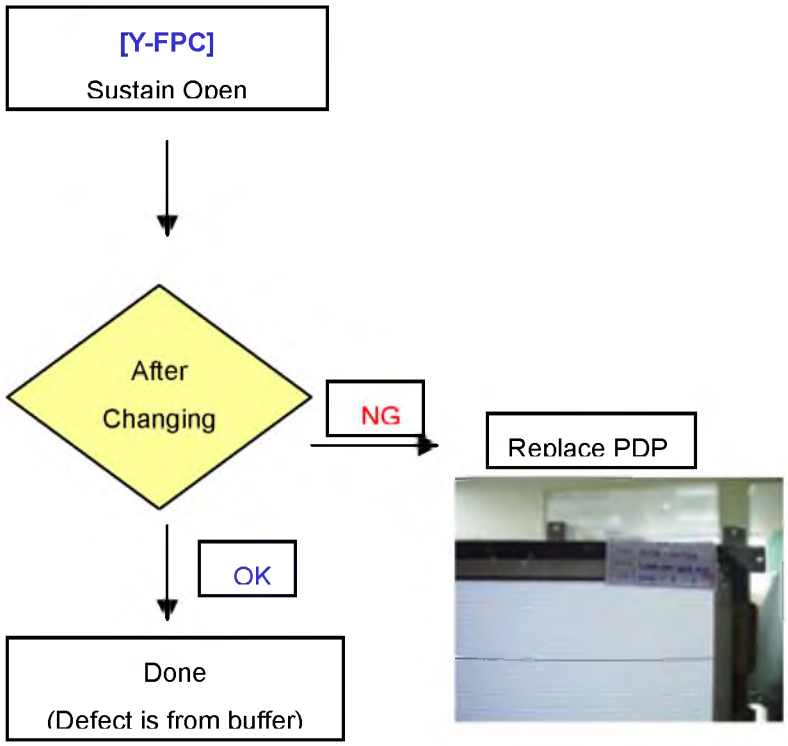
This page shows you how to check the boards, and the following pages show you how to find the defective board.



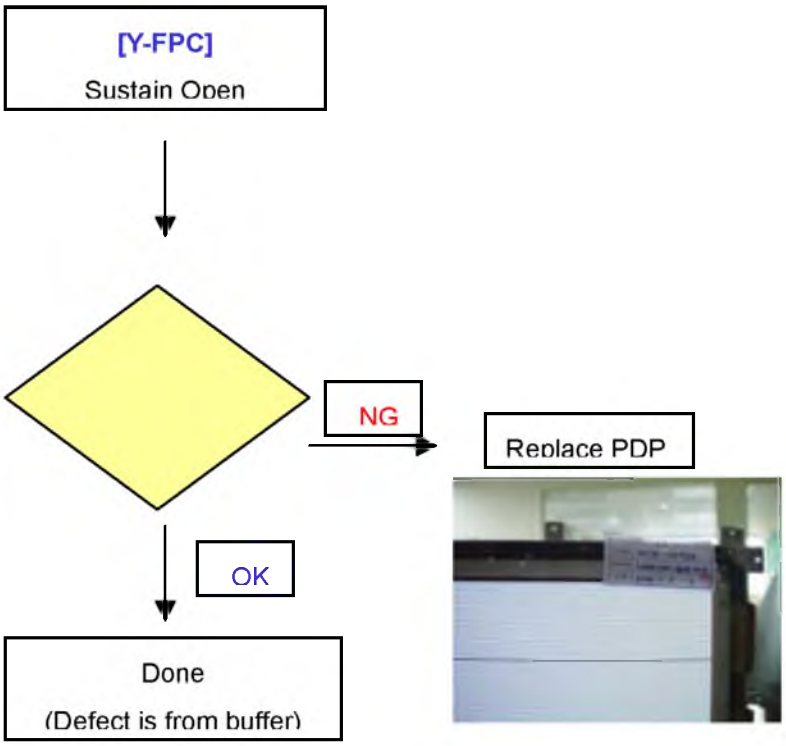

Y-Main
OK
Check
① F5001 for Vdd (5V)
② F5002 for Vcc (15V)
③ F5003 for Vs (170V)
Fuse
OPEN
Replace Y-B'd
OK
SHORT
Check
① Q5007/Q502
② Q5011/Q50112/Q5027
③ Q5009/Q5008/Q5030
④ Q5013/Q5014/Q5029
⑤ Q5018/Q5019/Q5028
FET
Replace
OK
X-Main
OK
Fuse
OPEN
Replace X-B'd
OK
SHORT
Check
① Q4004 /Q4005/Q4021
② Q4013/Q4019
③ Q4006/Q4020
④ Q4009/Q4010/Q4022
⑤ Q4014/Q4015
⑥ Q4016/Q4017/Q4023
FET
Replace X-B'd
OK
Logic



4-1-4 Sustain Open (some horizontal lines don't exist on screen)

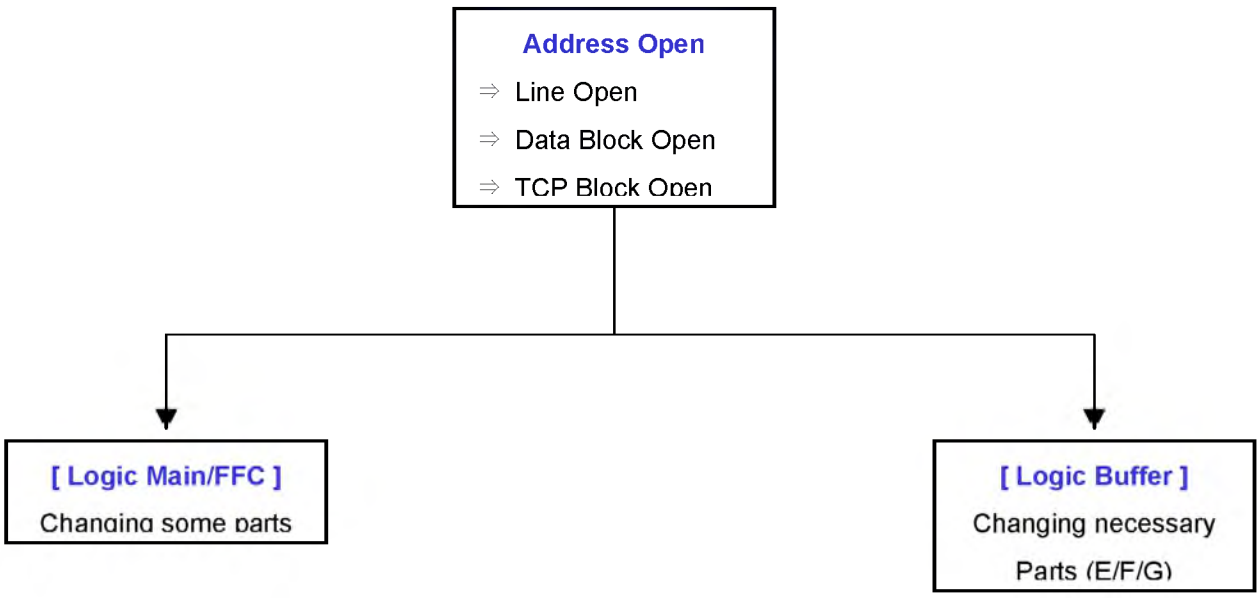


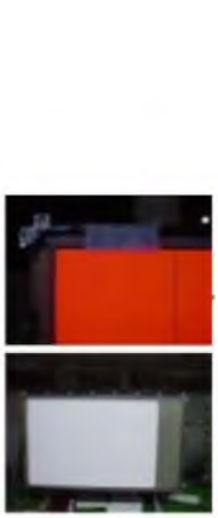
4-1-5 Sustain Short (some horizontal lines appear to be linked on Video)



4-1-6 Address Open (some vertical lines don't exist on screen)

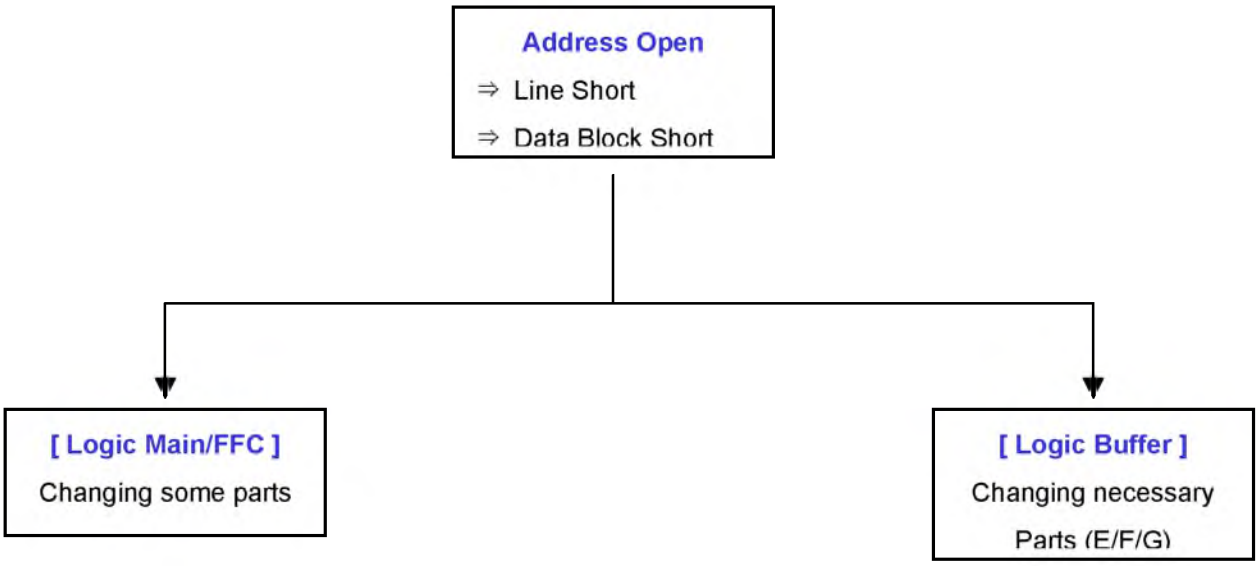
⇒ Address Open is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.

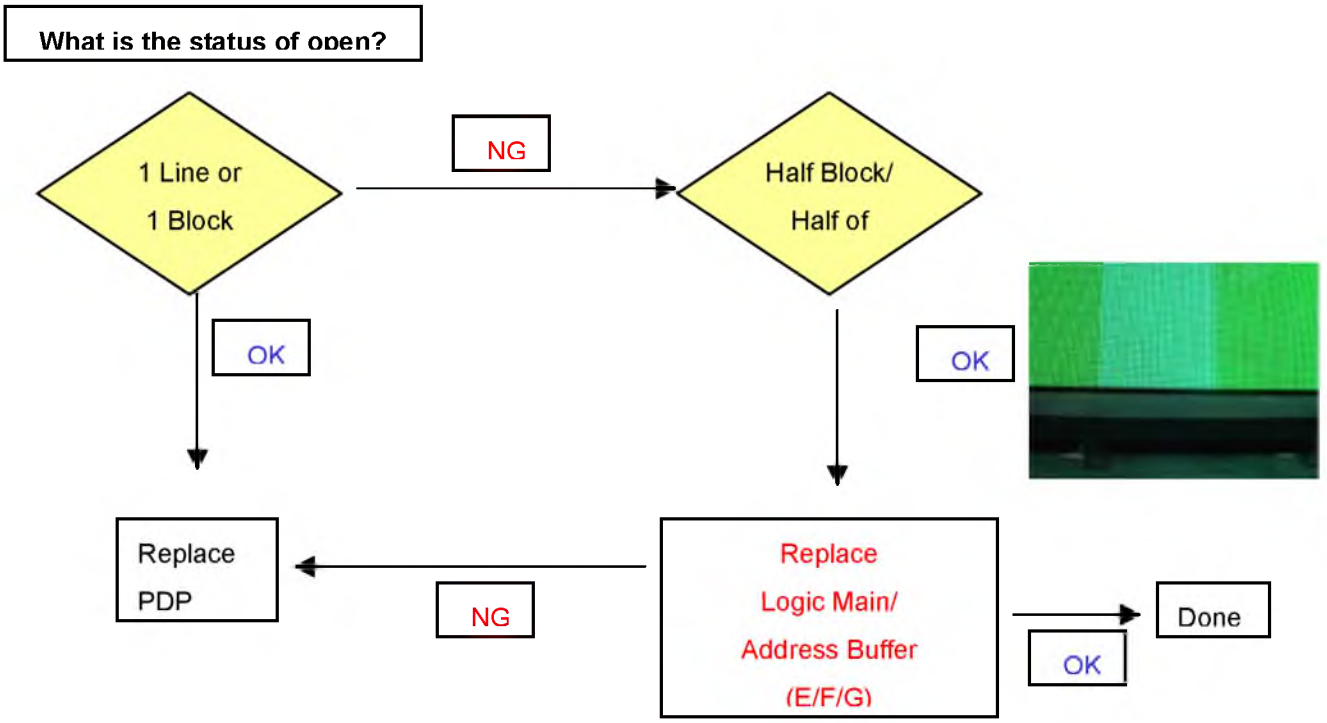




4-1-7 Address Short (some vertical lines appear to be linked on screen

⇒ Address Short is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.



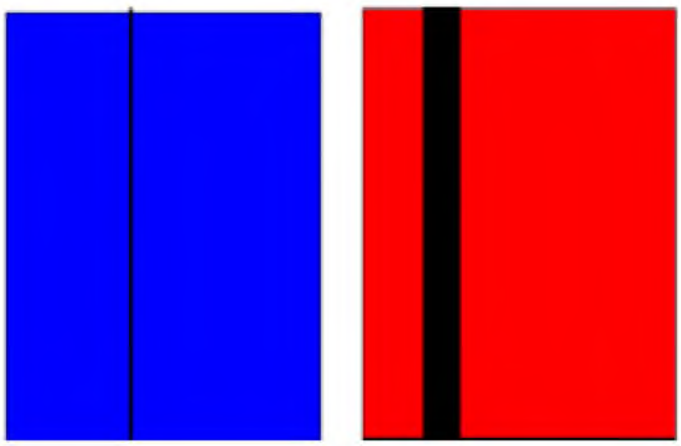


4-2 DEFECTS, SYMPTONS AND DETECTIVE PARTS

Condition Name	Description	Related Board
■ No Voltage Output	Operating Voltages don't exist.	PSU
■ No Display	Operating Voltages exist, but an Image doesn't exist on screen	Y-MAIN, X-MAIN, Logic Main, Cables
■ Abnormal Display	Abnormal Image(not open or short) is on screen.	Y-MAIN, X-MAIN, Logic Main
■ Sustain Open	some horizontal lines don't exist on screen	Scan Buffer, FPC of X / Y
■ Sustain Short	some horizontal lines appear to be linked on screen	Scan Buffer, FPC of X / Y
■ Address Open	some vertical lines don't exist on screen	Logic Main, Logic Buffer, FFC,TCP
■ Address Short	some vertical lines appear to be linked on screen	Logic Main, Logic Buffer ,FFC,TCP

◈ Defect: Address(vertical stripe) Open

■ Symptom : A line or block does not light up in address electrode direction.(1 line ,block open)



■Cause

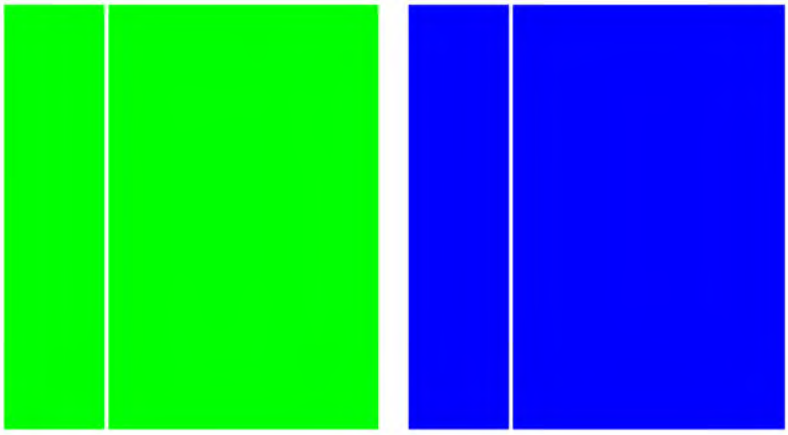
① manufacturing : Panel electrode single line/ foreign material./electrostatic/ TCP defect

② Parts : TCP, Board connection defect

③ Operation : Assembly error / Film damage

◈ Defect: Address(vertical stripe) Short

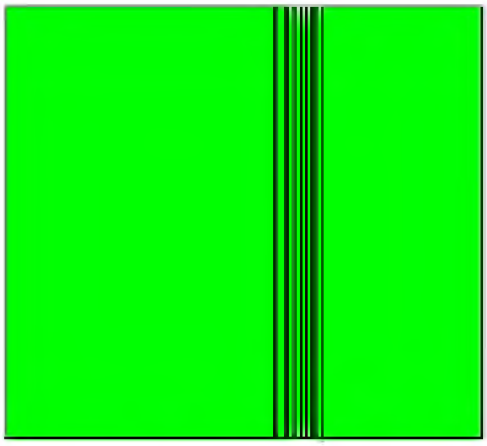
■ Symptom: Another color simultaneously appears because adjacent data recognizes the single pattern signal



■Cause

① manufacturing : Panel electrode short / Foreign material conductive foreign object inside TCP

② Part : TCP/buffer defect lighting electrode cutting defect

◈ Defect: Address output error	◈ Defect: Sustain(horizontal stripe) Open
■ Symptom.: A defect other than address open and short Data printout signal error occurring at certain Gradation or pattern  	■ Symptom : One or more line do not light up in Sustain direction  ■Cause : ① manufacturing : .Panel bus electrode single line FPC pressure defect ② Parts : FPC/board/connection disconnection ③ operation : assembly error.

◈ Defect: Sustain(horizontal stripe) Short

■Symptom : Combined or adjacent lines are short in sustain direction. The line appear brighter than other at Ramp gradation pattern or low gradation patter

■Cause

① manufacturing : Panel electrode short/Foreign material.

② Parts : Board/ connector/pin error

③ Operation : connector / assembling error

◈ Defect: Dielectric material layer damage

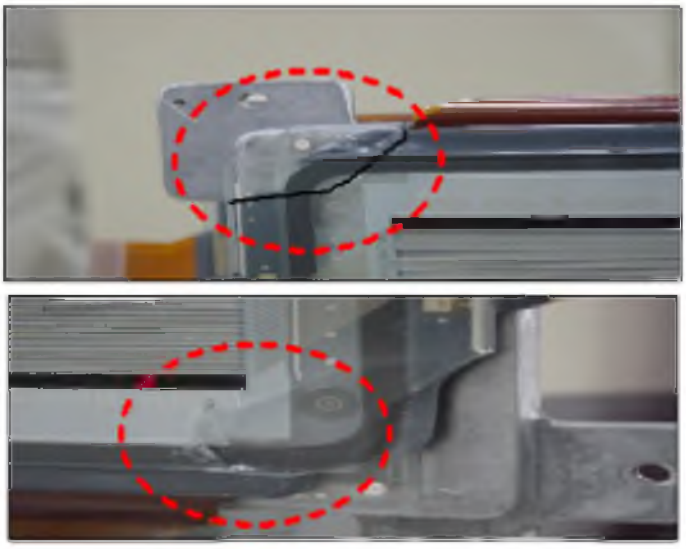
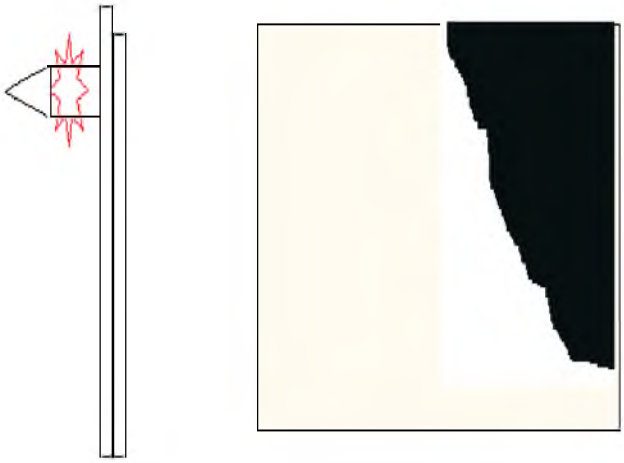
■ Symptom: Burn caused by the damage of address bus dielectric layer appears in the panel discharge/non discharge area. sustain also open/short occurs by the damage of address sustain printout

<Add Block and Line Open>

<Add and Sustain Open>

■Cause : layer uneven / abnormal voltage / foreign material repair failed

◈ Defext: F/White low discharge	◈ Defect: Weak discharge
■Symptom : Low discharge caused by unstable cells occurring at full white pattern if high (60 degree) or normal temparature.	■Symptom : Normal discharge but cells appear darker due to weak light emission occurring mainly at low (5 degree) Full white/Red/Green/Blue pattern or gradation pattern
 	 
■ Cause ① Panel : MgO source / dielectric thickness cell pitch/phosphor ② Circuit : drive waveform/ voltage condition	■ Cause ① Panel : MgO deposition count and thinckness / aging condition ② Circuit : drive waveform/ voltage condition

◈ Defect : panel damage	◈ Defect: Exhaust pipe damage
■ Symptom : Panel crack or break. No image appears in some cause depending on the damaged parts and damage level.  ■ Cause ① Manufacturing : Flatness/palette pin interruption ② Operation : overload of panel corner / careless handling ③ Panel : Flatness / assembly error	■ Symptom. : Crack in break if exhaust pipe an image is partially lacking or the panel noise occurs depending on the damaged parts and with the passage of time  ■ Cause : Careless panel handling

5. Disassembling / Assembling

5-1 Tools and measurement equipment

5-1-1. Tools

1) (+) type Screw Drivers : to screw the screws
2) Air Blower
3) Earth Ring
4) Small Driver : to adjust potentiometer
5) Dummy Discharge Resistor : 2.4kOhm/10W

5-1-2. Measuring Equipment

1) Oscilloscope : 500MHz sampling
2) Probe : 10:1
3) Digital Multi-meter
4) Signal Generator

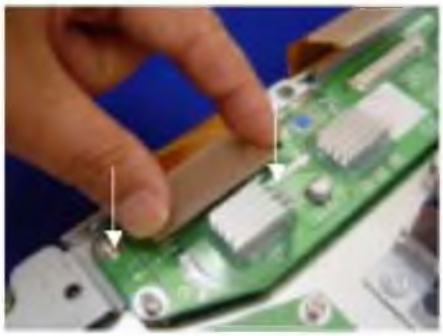
5-3 Disassembling & Re-assembling

5-3-1 Disassembling & Re-assembling of FPC (Flexible Printed Circuit) and Y-Buffer(Upper and Lower)

1. Removal procedures

1) Full out the FPC from Connector by holding the lead of the FPC with hands.

2. Assembling Procedures

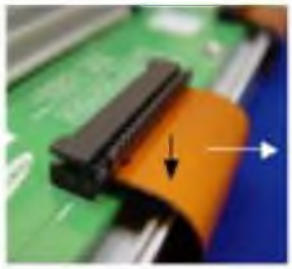


1) Push the lead of FPC with same strength until to be connected completely.

* Notice : Be careful do not get a damage on the connector pin during connecting by mistake.

5-3-2 Assembling & Disassembling of Flat Cable Connector of X-Main Board

1. Disassembling Procedure

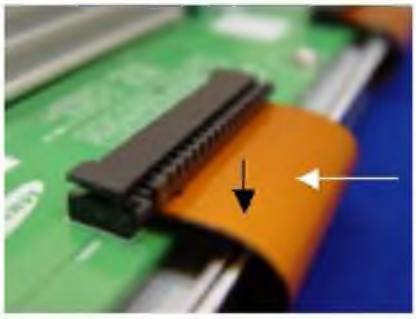


1) Pull out the clamp of connector.

2) Pull Flat cable out press down lightly.

3) Turn the Flat cable reversely.

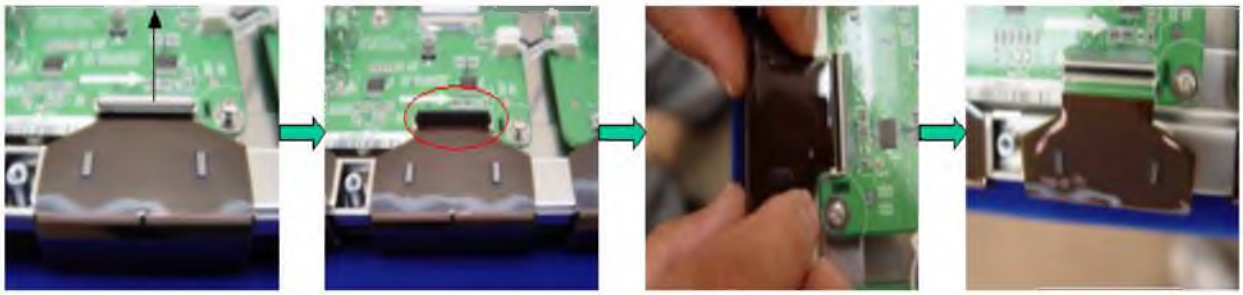
2. Assembling Procedure



1) Put the Flat cable into the connector press down lightly until locking sound (“Dack”) comes out.

5-3-3 Assembling & Disassembling the FFC and TCP from Connector

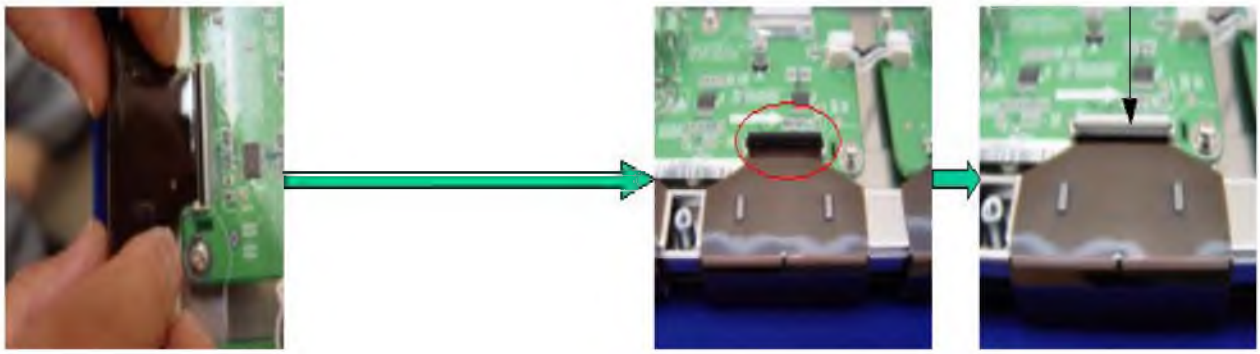
1. Disassembling of TCP



1) Open the clamp carefully.

2) Pull the TCP out from Connector.

2. Assembling of TCP



1) Put the TCP into the Connector carefully

2) Close the clamp completely.

(The sound (“ Dack”) comes out.)

* Notice : TCP and Connector was connected surely.

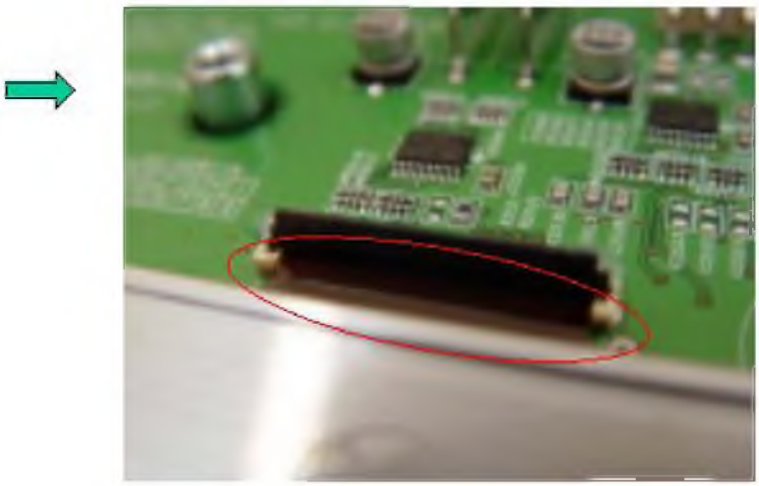
* Notice :

1) Checking whether the foreign material is on the Connector inside before assembling of TCP.

2) Be careful do not get a damage on the board by ESD during handling of TCP.

3. Misassembling of TCP

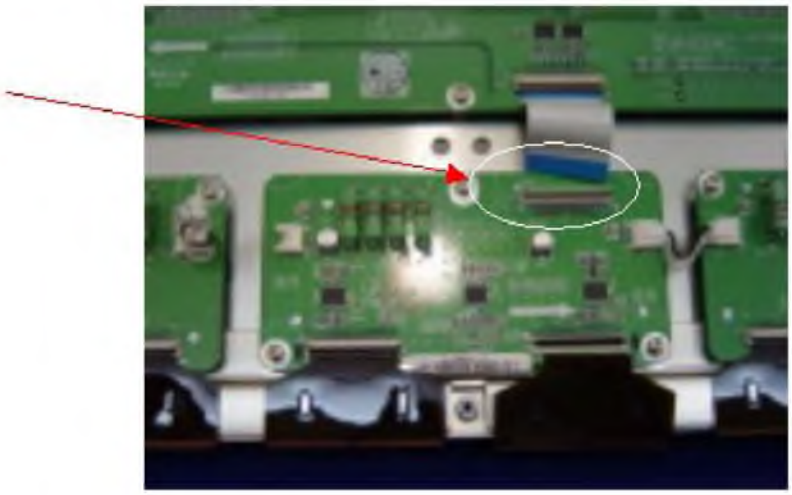
1) The misassembling of TCP is the cause of defect.



4. Checking method of misassembling of TCP

1)

5. Assembling & Disassembling of FFC

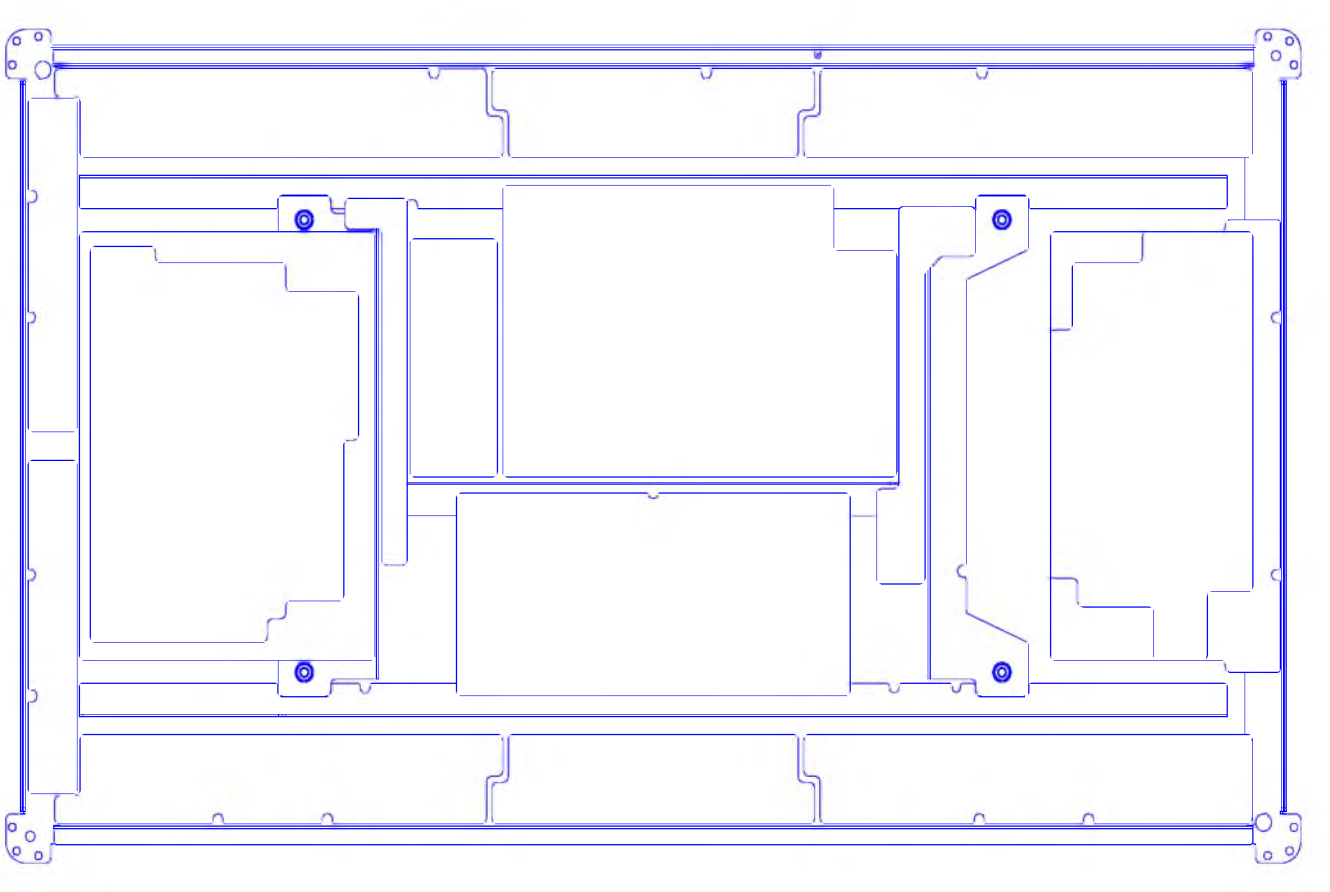


(This is the photo of the assembling of FFC)

The procedure of assembling and disassembling of FFC is the same as TCP.

5-3-4 Exchange of LBE, LBF, LBG board

(Photo 1)



(Photo 2)

1) Remove the screws in order of Center – Left Side – Right Side from heat sink and then get rid of heat sink. (Photo 1)
2) Remove the TPC, FFC and power cable from the connectors.
3) Remove all of the screws from defected board.
4) Remove the defected board.
5) Replace the new board and then screw tightly.
6) Get rid of the foreign material from the connector.
7) Connect the TCP,FFC and power cable to the connector.
8) Reassemble the TCP heat sink.
9) Screw in order of Right Side - Left Side - Center (Photo 2)

If you screw too tightly, it is possible to get damage on the Driver IC of TCP.

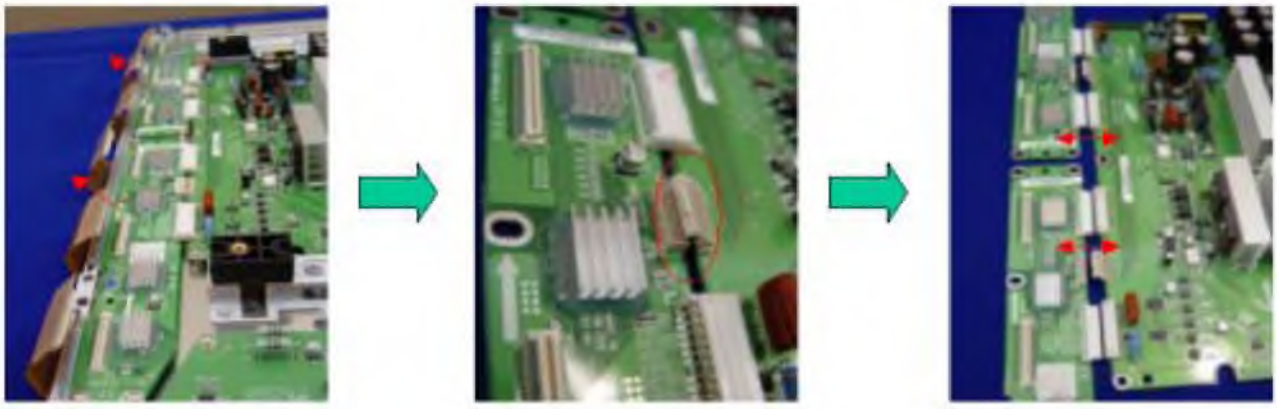
5-3-5 Exchange YBU, YBL and YM board

1) Separate all of the FPC connector of YBU (Y-Buffer upper) and YBL (Lower). (Photo 1)
2) Separate all of the connector of CN5001 and CN5008 from Y-Main.
3) Loosen all of the screws of YBU, YBL and YM.
4) Remove the board from chassis.

5) Remove the connector of CN5006 and CN5007 among YBU, YBL and YM.

6) Remove the YBL and YBU from Y-main.

7) Replace the defected board.



8) Reassemble the YBU and YBL to the Y-Main.

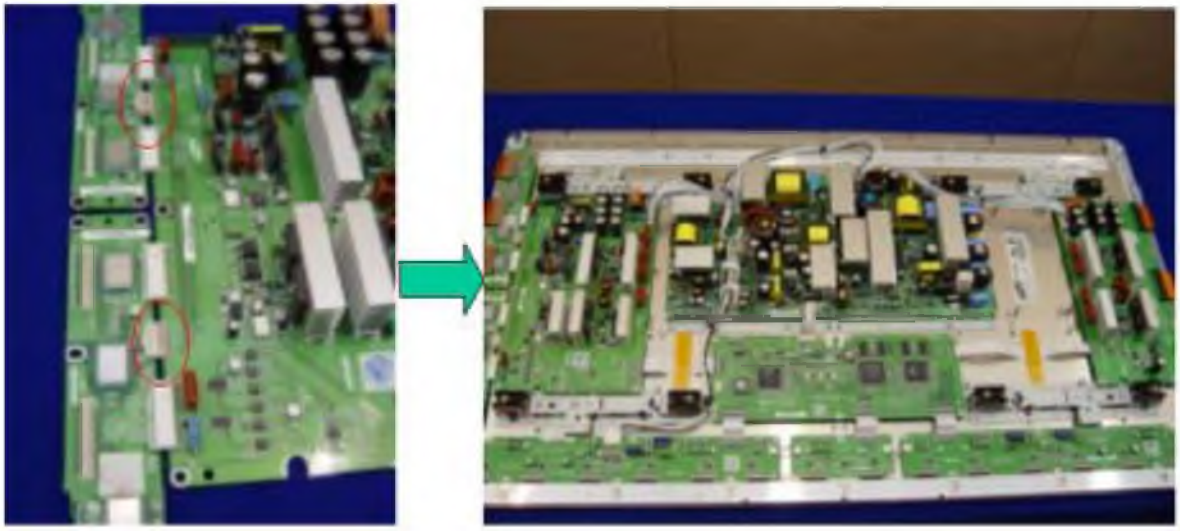
9) Connect the connector of CN5006 and CN5007 among YBU, YBL and YM.

10) Arrange the board on the chassis and then screw to fix.

11) Connect the FPC and YM of panel to the connector.

12) Supply the electric power to the module and then check the waveform of board.

13) Turn off the power after the waveform is adjusted.



6. Operation Check after Repair Service

6-1 Check Item

	Check Item	Specification	Remarks
Module assemble check	TCP Assembling condition	Securely connected or tightened	
	Drive board		
	Y BUFFER		
	Logic & Logic Buffer		
	Harness	Securely connected	
	Material Mixing	No material mixing	

6-2 Check Procedure

1) Visual check as following

a. Assembling condition of module.

b. No problem on the connection of module.

c. The grounding and easily short-circuited parts are not damaged.

2) Check the Dip Switch is setting [SW2000]

3) Turn on the power to PDP module, and then check that LED lights up and the SET is working well.

4) Check the power voltage after turn on the power, and then check the Display condition by tapping slightly the Y-FPC 2 or 3 times.

5) Check whether something wrong during Full White Pattern period.

6) If something wrong, each voltage should be set to the standard voltage by using Multi-Tester and adjusting tools.

7) Adjust the waveform, using Oscilloscope for the waveform adjusting point.

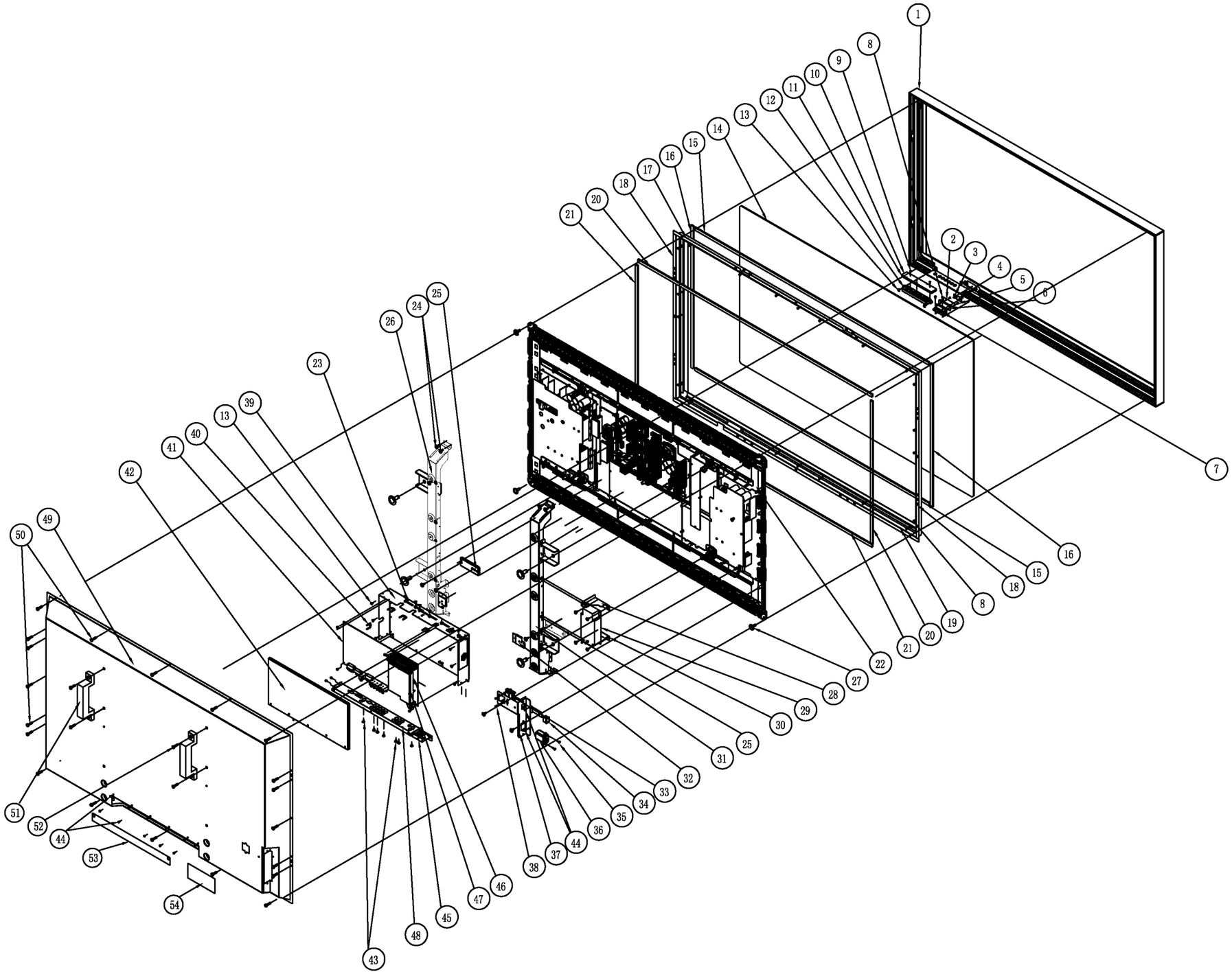
8) Check the discharge of front panel by changing the image for each pattern.

9) Check the Low-discharge, Over-discharge and panel condition by adjusting the Pattern Generator Level.

10) Discharge still remain send back to SDI

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER, DO NOT UPDATE MASTER MANUALLY

DWG.Rev.	ZONE	DESCRIPTION	DATE	REVISOR



ITEM	PART NO.	DESCRIPTION	QTY	REMARK
55				
54	387-50AD01-01H	MODEL PLATE AKAI ENG PDP5016H	5 H	
53	384-42D103-04H	PVC SHEET FOR E-ROOM PCB USA	1	
52	604-601020-00	MACH. SCREW MGX20	4	
51	248-46D201-01	HANDLE FOR PLASMA BLACK	2	
50	623-401812-00	TAPING SCREW B-TYPE TRUSS 4X12 B ZNP +H	24	
49	402-50SB02-01S	BACK COVER	1	
48	436-42D123-01S	TERMINAL SHEET	1	
47	483-42D104-01	SHIELD COVER RF	1	
46	481-42D105-01	SHIELD BOX RF	1	
45	426-50SB01-01S	AV2 BRACKET	1	
44	602-305006-00	PAN-WASHER 3X6 B ZNP =H	25	
43	614-300210-10	SCREW 3X10	7	
42	483-42D103-01	SHIELD COVER e-room	1	
41	E7801-056010	PCB ASSY MAIN 1VPC_DVI(HDCP)_CCD EROOM-SDI	1	
40	367-42D101-01	EDGE SADDLE 14MM	5	
39	481-42D105-01	SHIELD BOX E-ROOM	1	
38	614-300210-00	STP SCREW 3X10	7	
37	426-50SB0A-01S	POWER BRACKET STYLE B	1	ASM
36	E3219-002003	AC LINE FILTER	1	
35	601-305008-10	MACH. SCREW 3X8	2	
34	E4101-027001	SWITCH POW MR-22-N2BB-F2 ROCKET	1	
33	771-42AF01-01	SPK JACK PCB ASSY E-ROOM	1	
32	429-50SB06-01S	SHIELD BOX BRACKET		
31	420-50SB03-01S	MAIN BRACKET RIGHT	1	
30	424-50SB02-01S	POWER PCB BRACKER (B)	1	
29	E7801-057001	PCB ASSY SMPS 24/18V MPT012A	1	
28	424-50SB01-01S	POWER PCB BRACKER (A)	1	
27	60D-508012-40	W/SPRING WASHER M5.0X0.8X12MM WHITE ZIN/P	4	
26	420-50SB02-01S	MAIN BRACKET LEFT	1	
25	429-50SB0A-01S	CONNECT BRACKET	2	
24	60D-407010-10	MACH. SCREW W/SP WASHER 4X10	27	
23	457-42D101-01	CLAMP	10	
22	E6205-002003	DISPLAY PDP SDI-WXGA 50"	1	
21	326-064510-50	SPONGE CUSHION 645X10X5.0MM W/ADHESIVE	2	
20	326-115010-50	SPONGE CUSHION 1150X10X5.0MM W/ADHESIVE	2	
19	423-50SB07-01S	FILTER SUPPORT BTM	1	
18	423-50SB03-01S	FILTER SUPPORT L&R	2	
17	423-50SB06-01S	FILTER SUPPORT TOP	1	
16	553-067009-40A	670X9X4.0MM W/CONDUCTIVE ADHESIVE	2	
15	553-114009-40A	1140X9X4.0MM W/CONDUCTIVE ADHESIVE	2	
14	900-500101-01B	DISPLAY FILTER 50" OPTIMAX (116X87.1X3.2) (NK1-509-A003-E3-K2)	1	
13	602-305006-10	MACH-SCREW WHR 3X6	20	
12	277-42D101-XXS	FUNCTION KNOB	1	
11	771-42D105-01	KEY PCB ASSY FOR TD1/EROOM	1	
10	388-42D101-01	PC SHEET FOR KEY PCB	1	
9	614-260208-10	STP SCREW 2.6X8	3	
8	624-302406-10	TAP SCREW B-TYPE BINDING 3X6 WNC +H	22	
7	429-45AD07-01	REMOTE PCB BRACKET	1	
6	771-50SB03-01	IR RECEIVE PCB ASSY SB/EROOM	1	
5	604-305005-30	MACH.SCREW BID 3X5	2	
4	269-42D101-01L	REMOTE LENS	1	
3	263-42D101-01L	POWER LEN	1	
2	388-42P101-01	PC SHEET FOR REMOTE PCB	1	
1	400-50AD03-01	FRONT CABINET (AL) SILVER W/AKAI 50HAD	1	

DRAWN.						
CHECKED						
APPRD.						
3rd ANGLE PROJECTION						

TOLERANCE UNLESS OTHERWISE SPECIFIED

0 ~ 30	± 0.10
>30~100	± 0.20
>100	± 0.30
ANGULAR:	± 0.3°
UNIT :	mm

KAWA ELECTRONIC R & D CENTRE

MATL.

FINISH

TITLE PDP50HADSE-A01 Explode

MODEL NO. 50HAD

A2 | PART NO. EXP-50AD02-01 | DWG. NO.

SCALE NIL | SHEET 1 OF 1

Spare part list for PDP5016H

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
	PDP50HADSE-A01	AKAI PDP 50"(PDP5016H) SDI-XGA 100-240/50-60HZ USA SILVER			
1>	510-50AD01-01K	GIFT BOX AKAI ENG PD50HAD K	1.000000	Piece	K
2>	518-50AD11-01K	BOTTOM BOX	1.000000	Piece	K
3>	580-50AD01-03	INSTRUCTION BOOKLET E FOR 50HAD AKAI SDI/ E-ROOM	1.000000	Piece	K
4>	E7801-056010	PCB ASSY MAIN 1VPC_DVI(HDCP) _CCD EROOM-SDI	1.000000	SET	K
5>	E7801-056201	PCB ASSY TUNER NTSC	1.000000	Piece	K
6>	E7801-057001	PCB ASSY PSU 24/18V MPTO12A MEGMEET	1.000000	SET	K
7>	790-002514-A2	AKAI REMOTE ASSY 42KEYS 0025 USA SILVER	1.000000	SET	K
8>	244-34B811-01	GIFT BOX HANDLE 34B8	2.000000	Piece	S
9>	248-46D201-01	HANDLE FOR PLASMA BLACK	2.000000	Piece	S
10>	263-42D101-01L	POWER LENS 42D1 L	1.000000	Piece	S
11>	269-42D101-01L	REMOTE LENS 42D1 L	1.000000	Piece	S
12>	300-50P101-02C	POLYFOAM TOP 50TP1	1.000000	Piece	S
13>	300-50P102-02C	POLYFOAM BOTTOM 50TP1	1.000000	Piece	S
14>	310-111404-07V	POLYBAG 11"X14"X0.04 FV	1.000000	Piece	S
15>	310-633810-02T	POLYBAG 63"X38"X1.0MM W/ WARNING &RECYCLE MARK&HOLE	1.000000	Piece	S
16>	322-42P101-01	REMOTE LENS RUBBER SPACER PDP-42TP1	1.000000	Piece	S
17>	322-42P102-01	POWER LENS RUBBER SPACER PDP-42TP1	1.000000	Piece	S
18>	322-42P103-01	SEPARATE RUBBER SPACER FOR REMOTE AND POWER 42TP1	1.000000	Piece	S

19>	329-064510-50	SPONGE 645X10X5.0MM W/ ADHESIVE	2.000000	Piece	S
20>	329-115010-50	SPONGE 1150X10X5.0MM W/ ADHESIVE	2.000000	Piece	S
21>	384-42D103-04H	PVC SHEET FOR E-ROOM PCB USA	1.000000	Piece	S
22>	387-50AD01-01H	MODEL PLATE AKAI ENG PDP5016H H	1.000000	Piece	S
23>	388-42D103-01H	CAUTION PLATE ENG 42D1 H	1.000000	Piece	S
24>	388-42P101-01	PC SHEET FOR REMOTE PCB 42P1 94V0 0.25MM	1.000000	Piece	S
25>	388-42SB04-01H	POWER PLATE SANSUI 42SB H	1.000000	Piece	S
26>	388-50AD01-01H	SPEAKER PLATE FOR PDP50HAD	1.000000	Piece	S
27>	400-50AD03-01	FRONT CABINET (AL) SILVER W/ AKAI 50HAD	1.000000	Piece	S
28>	402-50SB02-01S	BACK COVER FOR 50" LG	1.000000	Piece	S
29>	424-50SB01-01S	POWER PCB BRACKER (A)	1.000000	Piece	S
30>	424-50SB02-01S	POWER PCB BRACKET (B)	1.000000	Piece	S
31>	426-50SB01-01S	AV2 BRACKET	1.000000	Piece	S
32>	426-50SB0A-01S	POWER BRACKET STYLE B	1.000000	Piece	S
33>	436-42D123-01S	TERMINAL SHEET FOR E-ROOM PCB USA 42D1 S	1.000000	Piece	S
34>	481-42D105-01	SHIELD BOX FOR USA RF 42D1	1.000000	Piece	S
35>	481-50SB11-01S	SHIELD BOX FOR E-ROOM 50SB S	1.000000	Piece	S
36>	483-42D103-01	SHIELD COVER FOR E-ROOM PCB 42D1	1.000000	Piece	S
37>	483-42D104-01	SHIELD COVER TOP FOR 42D1	1.000000	Piece	S
38>	486-50AD01-01	NAME PLATE AKAI SIL/BLACK 50AD	1.000000	Piece	S

39>	511-42D102-01A	ACCESSORY BOX	1.000000	Piece	S
40>	553-002509-40A	EMI SHIELD GASKET 25X9X4.0MM W/CONDUCTIVE ADHESIVE	4.000000	Piece	S
41>	553-005009-25A	SHIELD GASKET 50X9X2.5MM W/ CONDUCTIVE ADHESIVE KI JD-60	2.000000	Piece	S
42>	553-006509-40A	SHIELD GASKET 65X9X4.0MM W/ CONDUCTIVE ADHESIVE KI JD-60	4.000000	Piece	S
43>	553-015009-40A	EMI SHIELD GASKET 150X9X4.0MM W/CONDUCTIVE ADHESIVE	8.000000	Piece	S
44>	553-020009-40A	SHIELD GASKET 200X9X4.0MM W/ CONDUCTIVE ADHESIVE KI JD-60	2.000000	Piece	S
45>	553-024509-40A	SHIELD GASKET 245X9X4.0MM W/ CONDUCTIVE ADHESIVE KI JD-60	2.000000	Piece	S
46>	553-026009-40A	EMI SHIELD GASKET 260X9X4.0MM W/CONDUCTIVE ADHESIVE	2.000000	Piece	S
47>	553-028009-40A	EMI SHIELD GASKET 280X9X4.0MM W/CONDUCTIVE	2.000000	Piece	S
48>	553-039509-10A	SHIELD GASKET 395X9X1.0MM W/ CONDUCTIVE ADHESIVE	1.000000	Piece	S
49>	553-067009-40A	EMI SHIELD GASKET 670X9X4.0MM W/CONDUCTIVE ADHESIVE	2.000000	Piece	S
50>	553-114009-40A	EMI SHIELD GASKET 1140X9X4.0MM W/CONDUCTIVE ADHESIVE	2.000000	Piece	S
51>	554-090030-01	SHIELD CLOTH 90X30MM W/ CONDUCTIVE ADHESIVE	1.000000	Piece	S
52>	563-119-	SERIAL NO. LABEL	1.000000	Piece	S
53>	568-P46T02-02	WARNING LB ENG 42SF NIL	1.000000	Piece	S
54>	579-42D103-02	ON/OFF LB ENG 42D1 NIL	1.000000	Piece	S
55>	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
56>	579-50AA02-01	DANGER CAUTION LABEL	1.000000	Piece	S
57>	579-50AD01-01	BAR CODE LABEL AKAI W/SERIAL NO PD50HAD(USA)	2.000000	Piece	S

58>	579-50AD02-01	SERIAL NO/BAR CODE LABEL 50HA (USA)	1.000000	Piece	S
59>	590-50AD01-01	WARRANTY CARD ENG AKAI PDP5006H	1.000000	Piece	S
60>	734-BM0304-02	SECC STAND BASE 50" W/ PACKING BIG BOX NIL SILVER (ESI)	1.000000	SET	S
61>	786-SW0411-01	AKAI WOOD SPEAKER ASSY W/ POLYFOAM SILVER FOR 50HAD (ESI)	1.000000	SET	S
62>	900-500101-01B	DISPLAY FILTER 50" OPTIMAX (1155X671X3.2)(NK1-50B-AD03-X2-A2)	1.000000	Piece	S
63>	E3213-011001	SOCKET ANT F/RCA	1.000000	Piece	S
64>	E3219-002003	EI I LET EMI FILTER WIT WIRES IOSSI-R-Q(B) HIGH&LOW	1.000000	Piece	S
65>	E3404-157004	AC CORD UL 1.88M (YY-3/ST3 YUNBIAO)	1.000000	Piece	S
66>	E3421-926031	WIRE ASSY 2.5 11P/11P FOR (SDI 50" L=190MM) (W/EMI)	1.000000	Piece	S
67>	E3421-926032	WIRE ASSY 2.5 10P/7P+3P FOR (SDI 50" L=400MM) (W/EMI)	1.000000	Piece	S
68>	E3421-926033	WIRE ASSY L=220MM 31P(SDI 50") (LVDS W/EMI)	1.000000	Piece	S
69>	E3421-926034	WIRE ASSY POWER CABLE 2Y/ L=300MM FOR (SDI 50") (W/EMI)	1.000000	Piece	S
70>	E3421-927006	WIRE ASSY AMP/AMP -2Y/550 (FROM SWITCH POWER) FOR SDI	1.000000	Piece	S
71>	E3421-927021	WIRE ASSY L=300MM 3WIRES FOR 42EAA POWER CONNECT W/ EMI	1.000000	Piece	S
72>	E4101-027001	SWITCH POW MR-22-N2BB-F2 ROCKET	1.000000	Piece	S
73>	E6205-002003	DISPLAY PDP 50" SDI-V3.0 (XGA) (127CM) COF S50HW-XDO3	1.000000	Piece	S
74>	E7301-011002	BATTERY AA R6P1.5V <2>	2.000000	Piece	S
75>	771-42AF01-01	SPK JACK PCB ASSY E-ROOM	1.000000	SET	S
76>	771-42D105-01	KEY PCB ASSY FOR TD1/EROOM	1.000000	SET	S
77>	771-50SB03-01	IR RECEIVE PCB ASSY SB/EROOM	1.000000	SET	S

If you forget your V-Chip Password

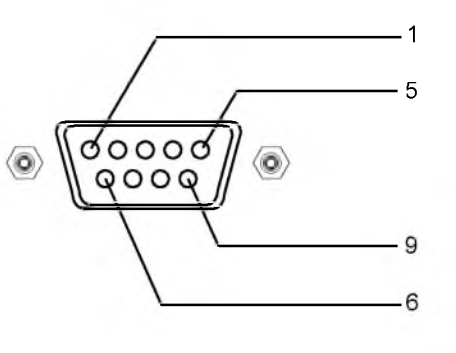
- Omnipotence V-Chip Password: **1234**.
- Press **MENU** button.
- Press **Up, Down** and CH+, CH-buttons to highlight "V-Chip" Control.
- Press OK button to pop up "INPUT PASSWORD".
- Use the Number buttons (0~9) to enter the omnipotence Password 1234.
- Press Down to highlight "Password change" Control.
- Press **OK** button to confirm and will pop up "Password Change" item.
- Change to your familiar Password again.

Software upgrade

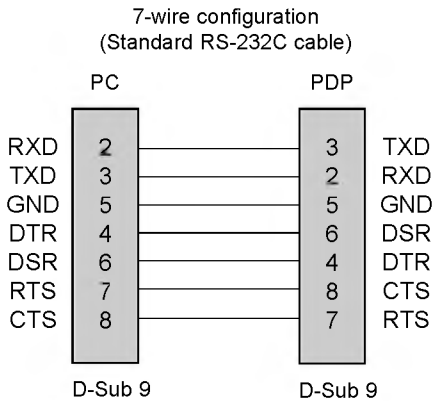
- Connect the RS-232C input jack to an external control device (such as a computer) and software upgrade.

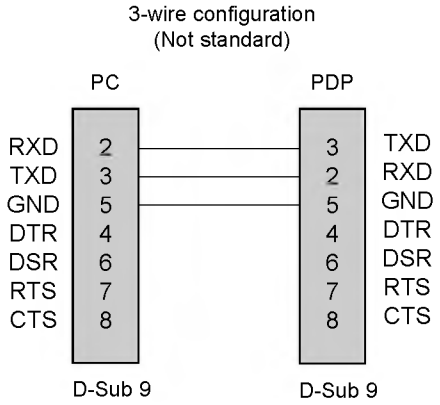
Type of connector; D-Sub 9-pin male

No.	Pin name
1	No connection
2	RXD (Receive data)
3	TXD (Transmit data)
4	DTR (DTE side ready)
5	GND
6	DSR (DCE side ready)
7	RTS (Ready to send)
8	CTS (Clear to send)
9	No Connection



RS-232C configurations





Software upgrade Process

- Power Switch OFF.
- Connect the serial port of the control device to the RS-232 jack on the PDP back panel.
  RS-232C connection cables are not supplied with the PDP.
- Power Switch ON. The power indicator on the front of the panel should now display red, means that the PDP is in standby mode.
- Copy the software (Flash Upgrader) to the computer.
- Open the software (Flash Upgrader.exe)
- Point "Flash" on the interface of the Flash Upgrader.exe.
- Press STANDBY button on the front panel or POWER button of Remote control, Power indicator green, the PDP is in power ON mode, software start upgrader immediately.
- Waiting for the upgrader programing, when it is finished, the PDP will auto power on.
- After the upgrader is finished, shut down the power switch, take out the RS-232C connection after the power indicator is extinguished.

Note: The computer and PDP must be keep **Power ON** in the software upgrade processing.